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Kanno et al.

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(45) **Date of Patent: *Sep. 6, 2016**

(54) **THREE-DIMENSIONAL RESISTIVE MEMORY DEVICE WITH ADJUSTABLE VOLTAGE BIASING**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 25 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/305,371**

(22) Filed: **Jun. 16, 2014**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Provisional application No. 61/935,232, filed on Feb. 3, 2014.

(51) **Int. Cl.**
G11C 13/00 (2006.01)
H01L 27/24 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 13/0069*** (2013.01); ***G11C 13/0002*** (2013.01); ***G11C 13/0023*** (2013.01); ***H01L 27/249*** (2013.01); *G11C 2213/71* (2013.01)

(58) **Field of Classification Search**
CPC G11C 2213/71; G11C 13/0069; G11C 13/0023; G11C 13/0002; H01L 45/1233
See application file for complete search history.

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Primary Examiner — Pho M Luu
Assistant Examiner — Jerome Leboeuf
(74) *Attorney, Agent, or Firm* — Oblon, McClelland, Maier & Neustadt, L.L.P.

(57) **ABSTRACT**

A semiconductor memory device according to an embodiment includes a memory cell array and a control circuit. The memory cell array includes: a plurality of first conductive layers that are stacked; a memory layer provided on a side surface of the plurality of the first conductive layers; and a second conductive layer that contacts the side surface of the plurality of the first conductive layers via the memory layer. A thickness of the first conductive layer disposed at the first position is larger than a thickness of the first conductive layer disposed at the second position. The control circuit is configured to apply a first voltage to a selected first conductive layer. The control circuit changes a value of the first voltage based on a position of the selected first conductive layer.

5 Claims, 20 Drawing Sheets

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FIG. 1

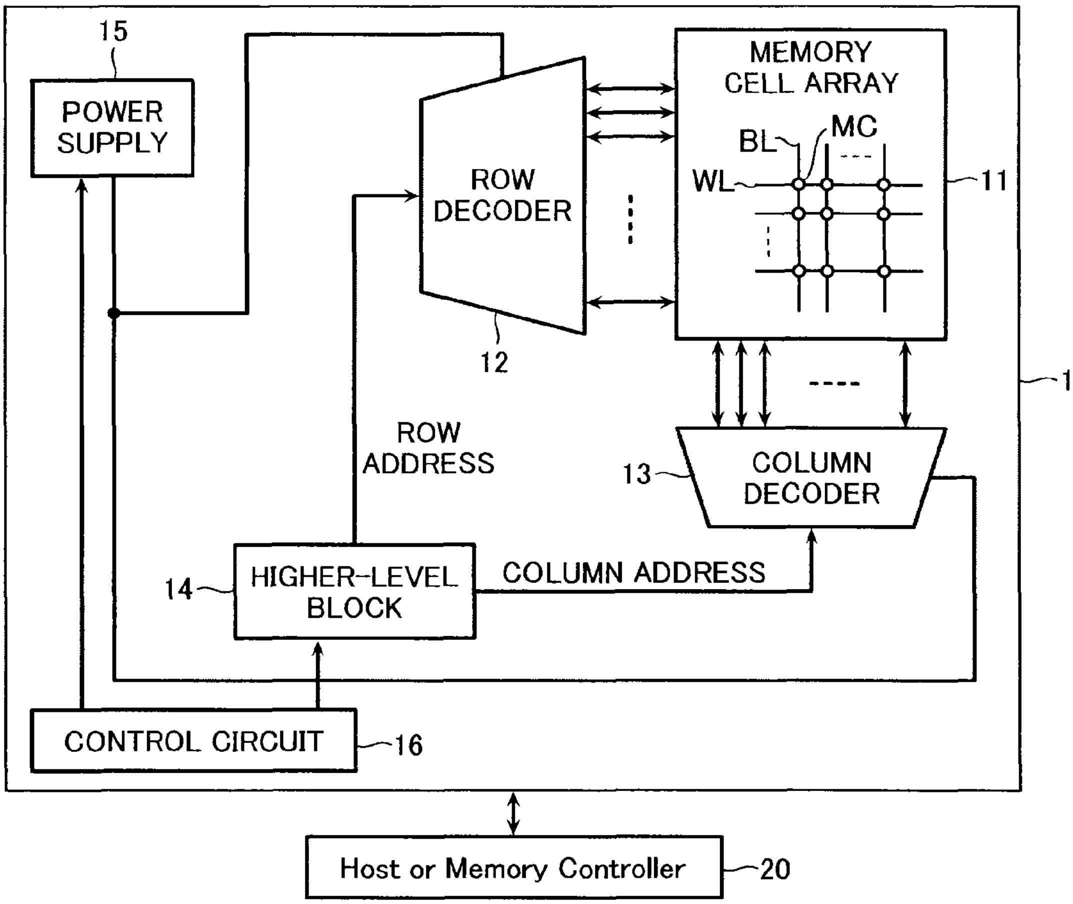

15
POWER SUPPLY
ROW DECODER
12
MEMORY CELL ARRAY
BL
MC
WL
11
1
ROW ADDRESS
13
COLUMN DECODER
14
HIGHER-LEVEL BLOCK
COLUMN ADDRESS
CONTROL CIRCUIT
16
Host or Memory Controller
20

FIG. 2

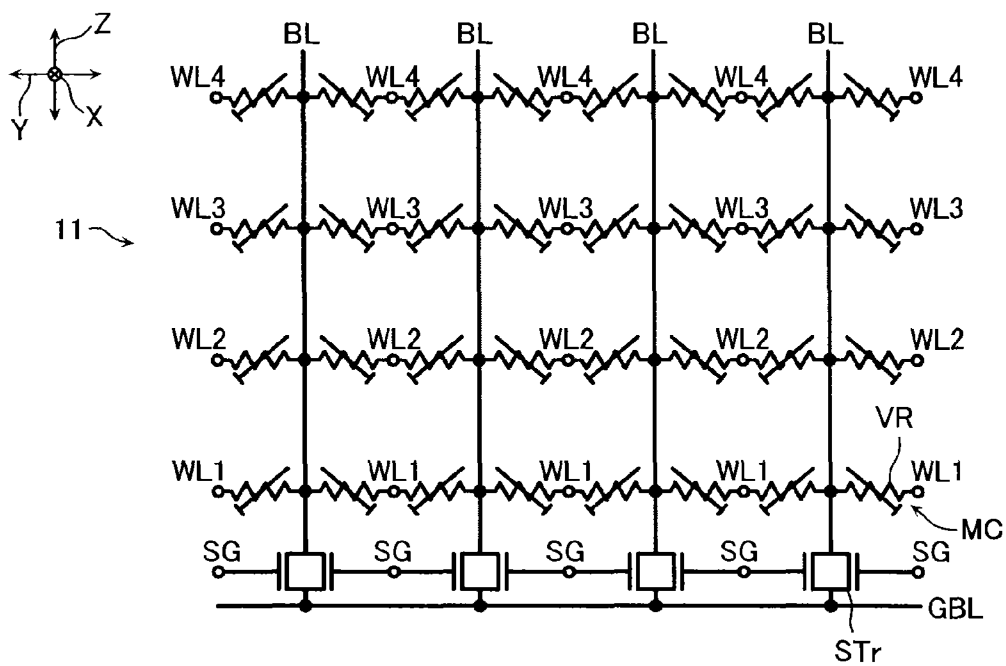

Z
Y
X
11
BL
WL4
WL3
WL2
WL1
VR
MC
SG
GBL
STr

FIG. 3

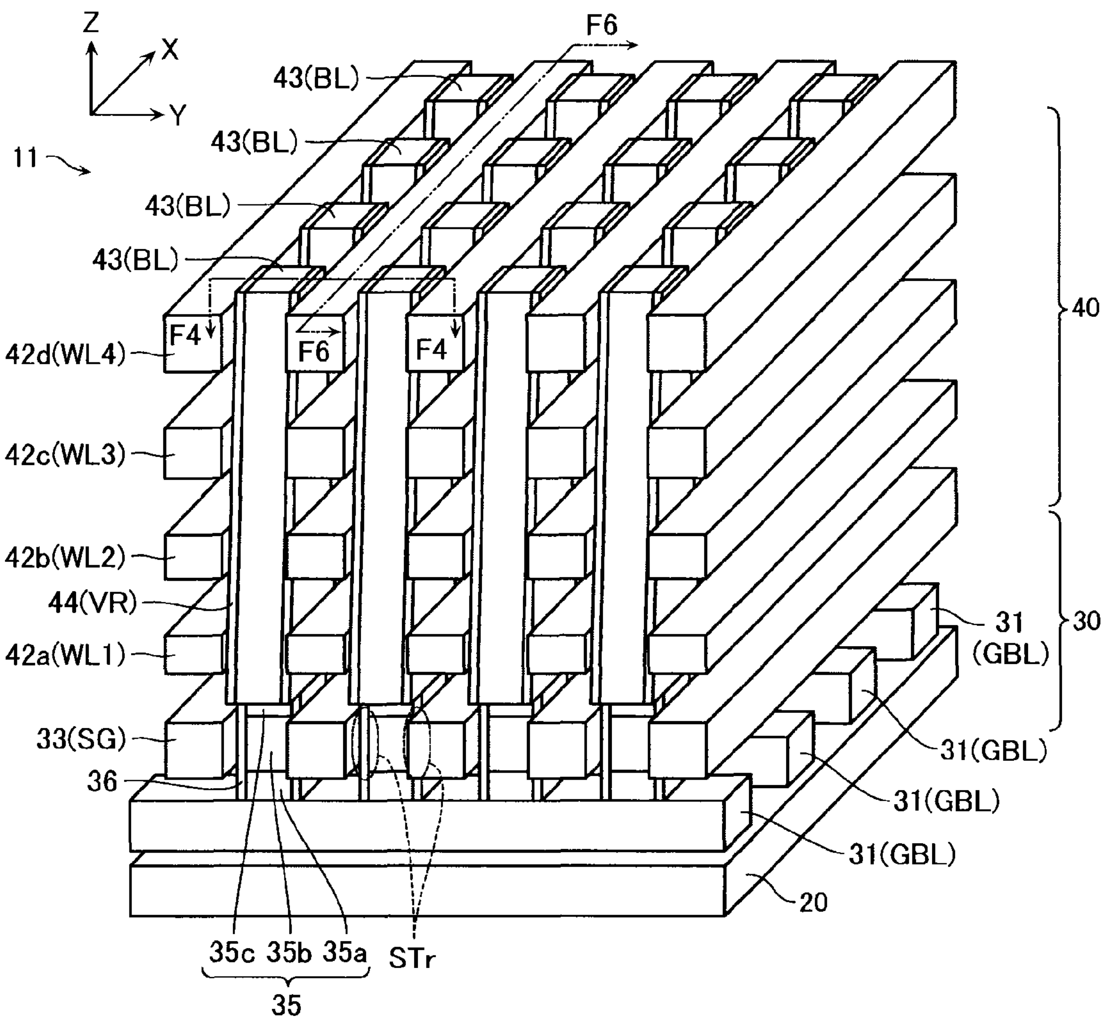

Z
X
Y
11
F6
43(BL)
43(BL)
43(BL)
43(BL)
F4
F6
F4
42d(WL4)
42c(WL3)
42b(WL2)
44(VR)
42a(WL1)
33(SG)
36
40
30
31
(GBL)
31(GBL)
31(GBL)
31(GBL)
20
35c 35b 35a
STr
35

FIG. 4

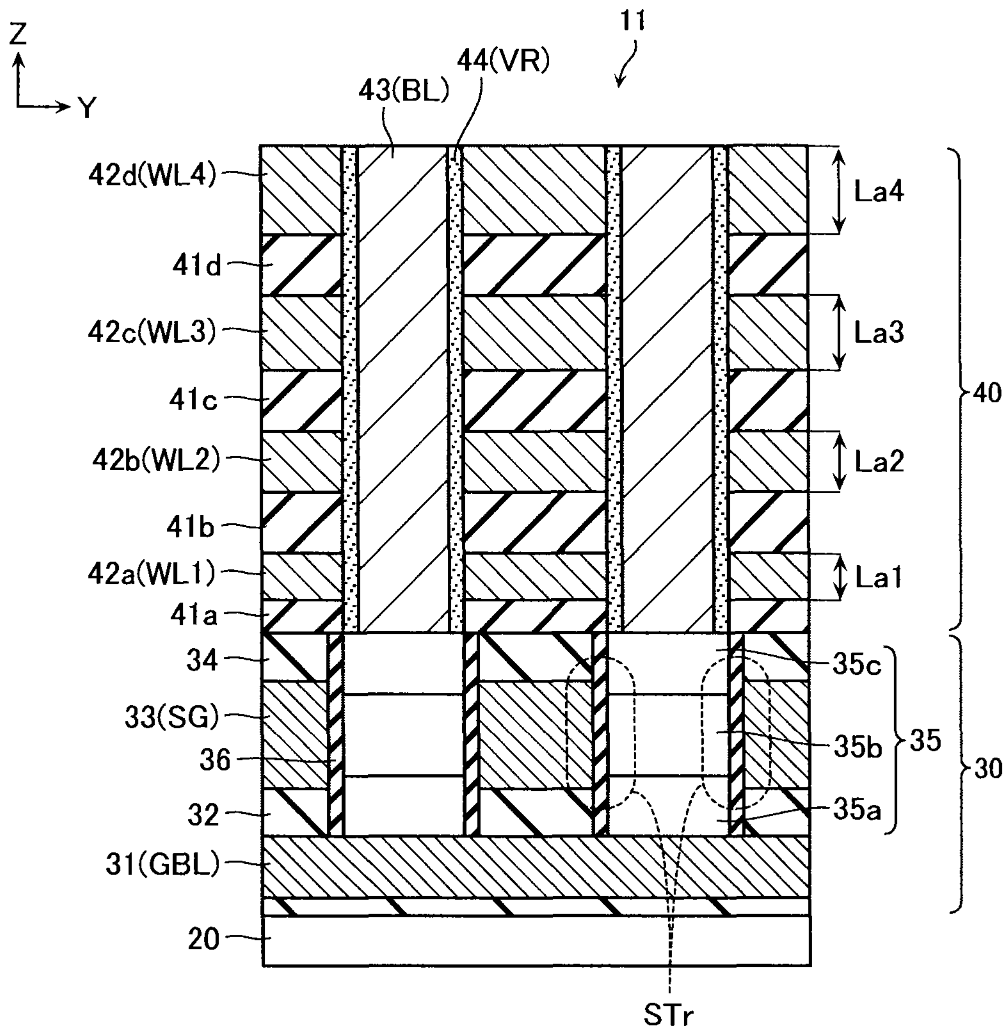

Z
Y
11
44(VR)
43(BL)
42d(WL4)
41d
42c(WL3)
41c
42b(WL2)
41b
42a(WL1)
41a
34
33(SG)
36
32
31(GBL)
20
La4
La3
La2
La1
40
35c
35b
35
35a
30
STr

FIG. 5

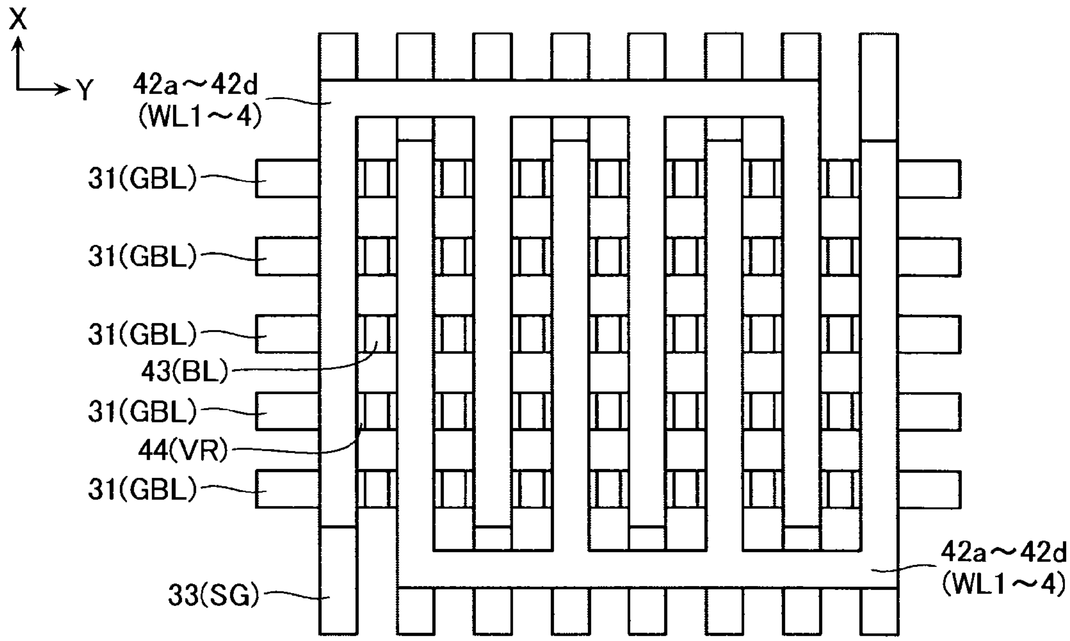

X
Y
42a～42d
(WL1～4)
31(GBL)
31(GBL)
31(GBL)
43(BL)
31(GBL)
44(VR)
31(GBL)
33(SG)
42a～42d
(WL1～4)

FIG. 6


Z
X
MC
43(BL1)
43(BL2)
43(BL3)
43(BL4)
42d(WL4)
Xa4
La4
42c(WL3)
Xa3
La3
42b(WL2)
Xa2
La2
42a(WL1)
Xa1
La1

FIG. 7

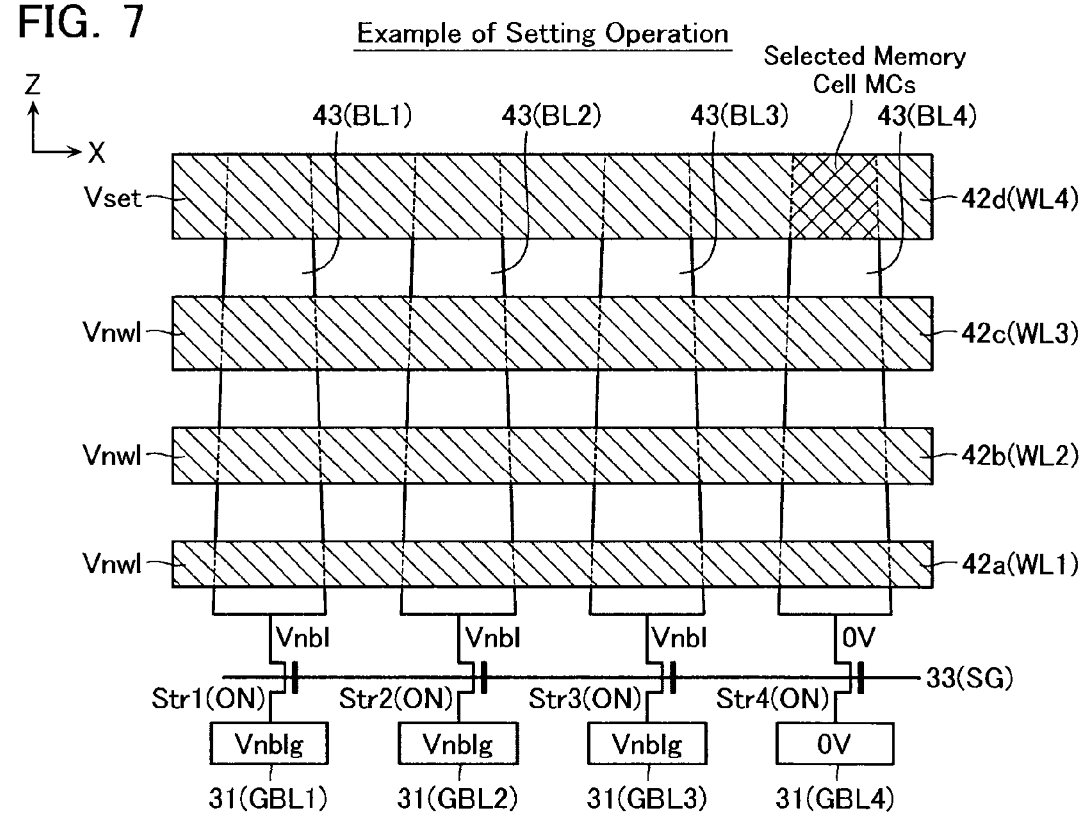

Example of Setting Operation
Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vset
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 8

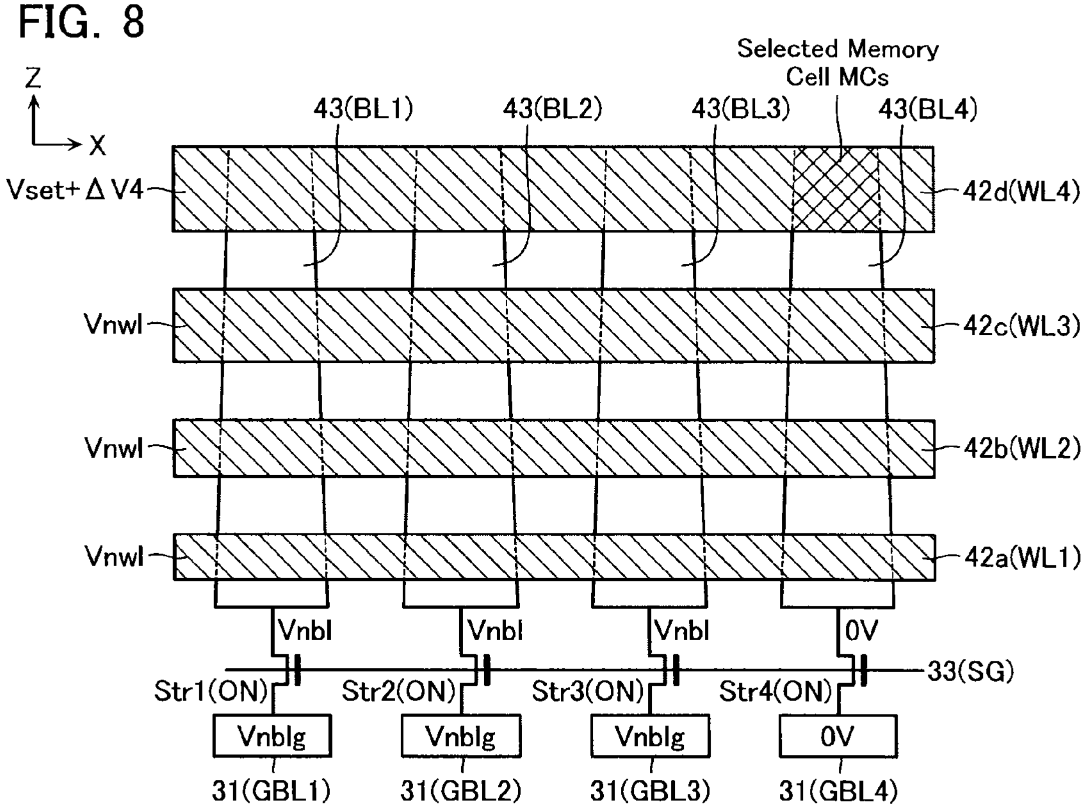

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vset+ΔV4
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 9

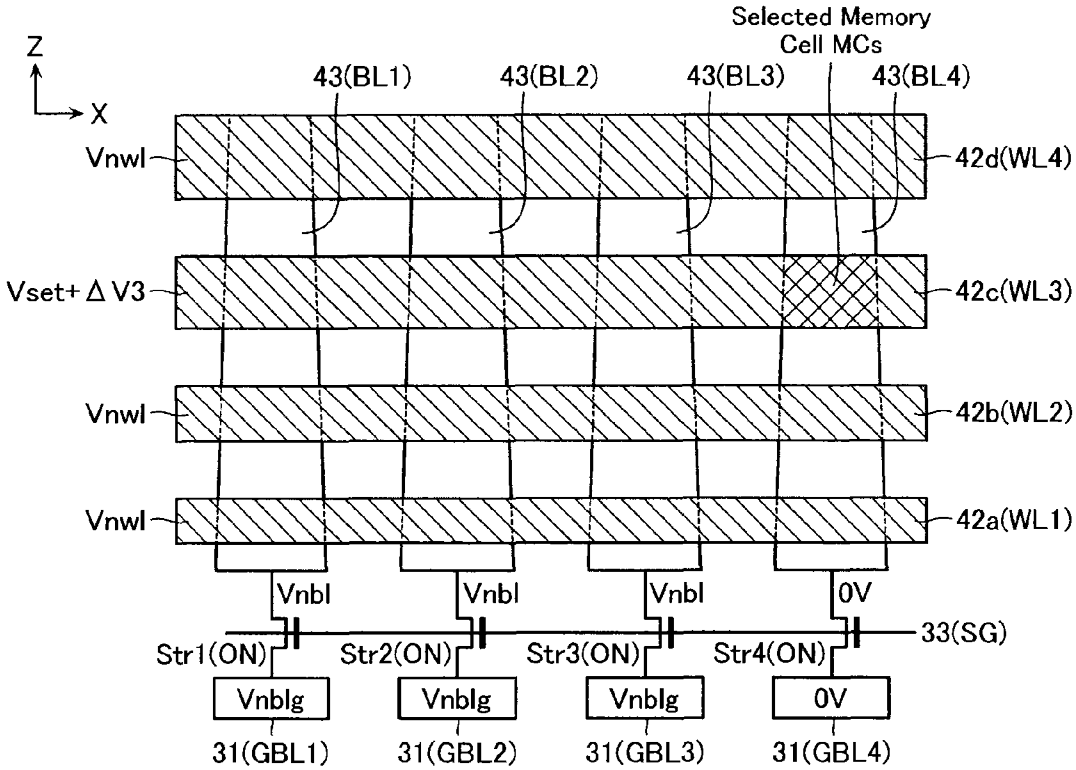

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vset+ΔV3
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 10

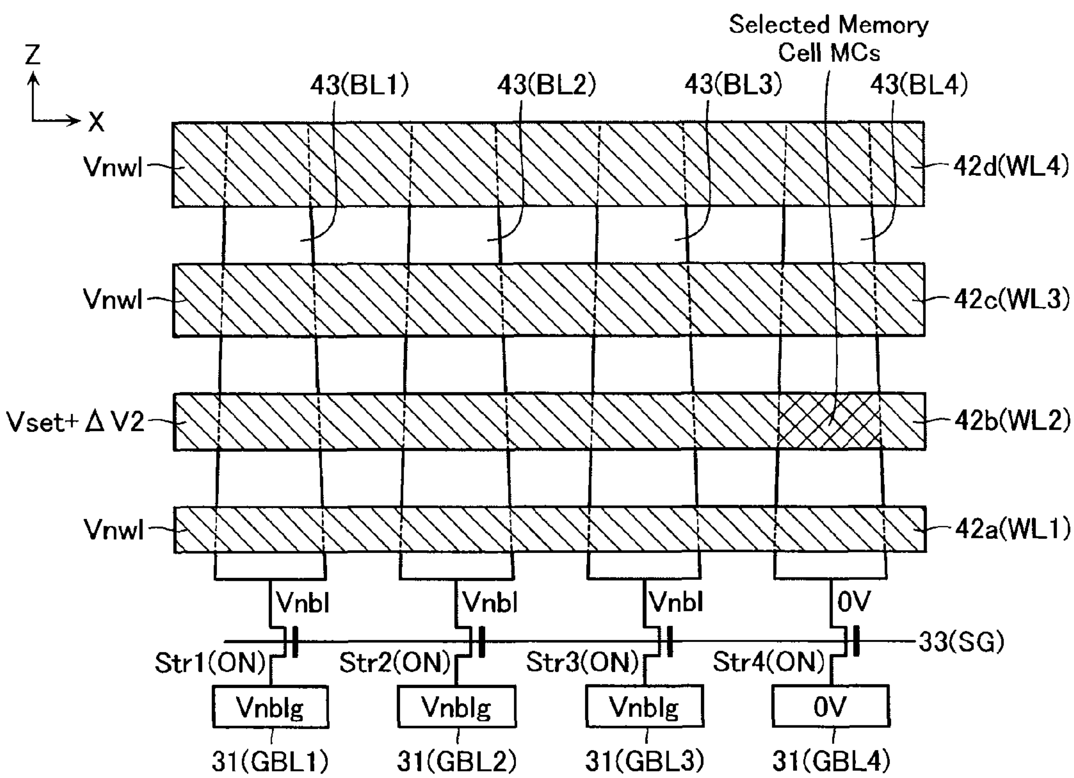
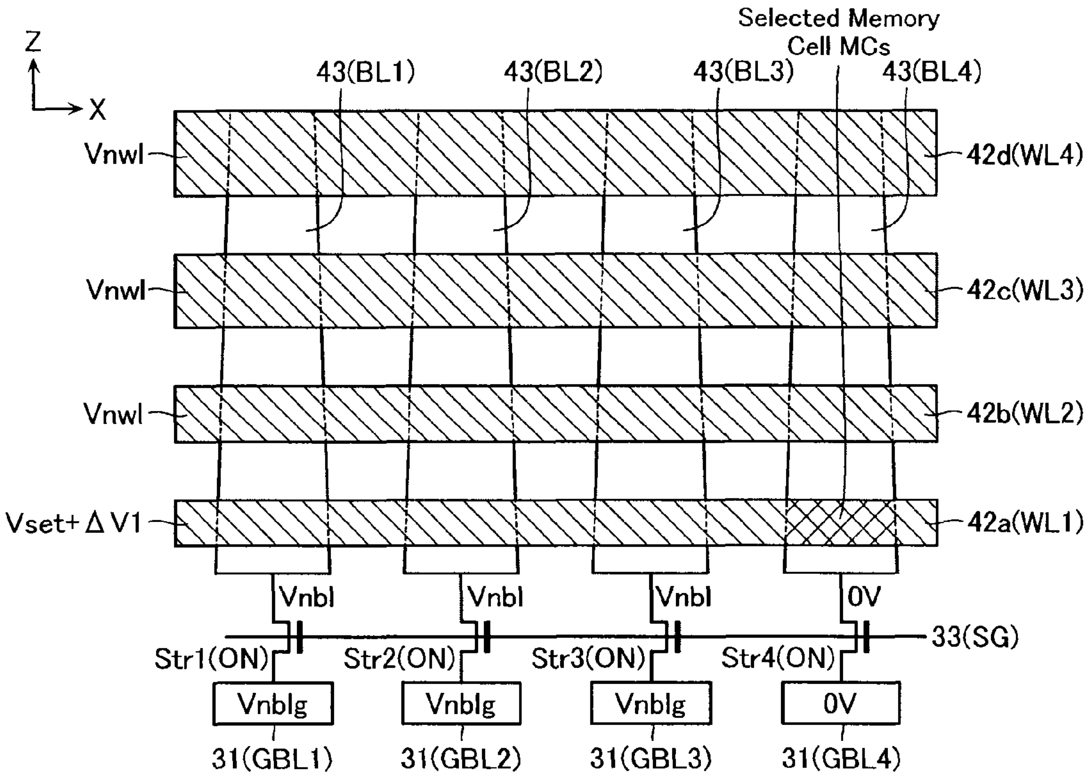
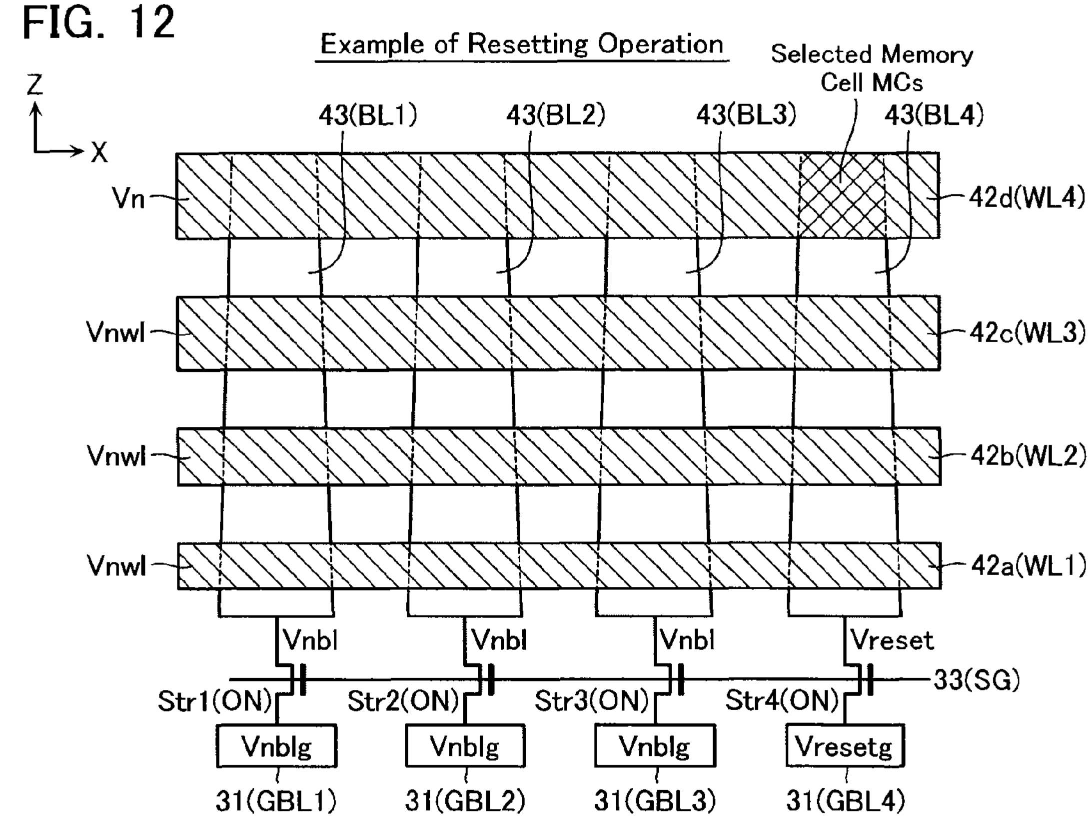

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vnwl
42c(WL3)
Vset+ΔV2
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 11



Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
Vnwl
Vnwl
Vset+ΔV1
42d(WL4)
42c(WL3)
42b(WL2)
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 12



Example of Resetting Operation
Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vn
Vnwl
Vnwl
Vnwl
42d(WL4)
42c(WL3)
42b(WL2)
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 13

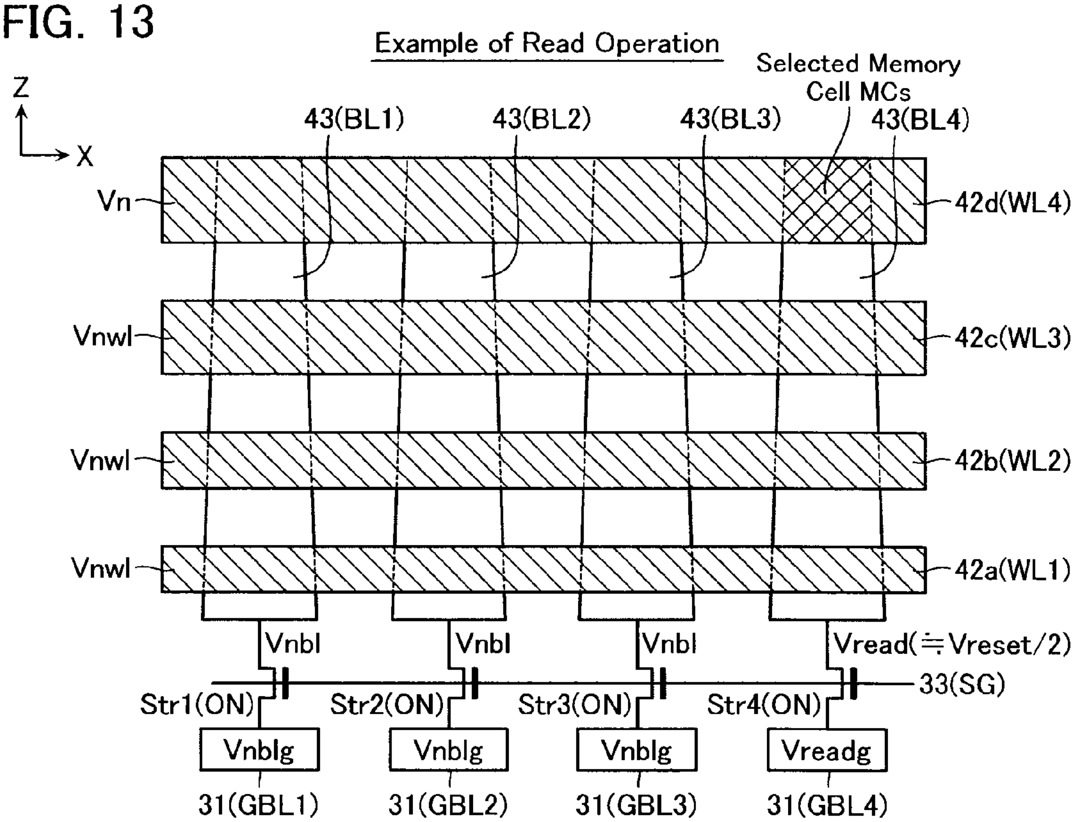

Example of Read Operation
Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vn
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vread(≒Vreset/2)
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vreadg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 14

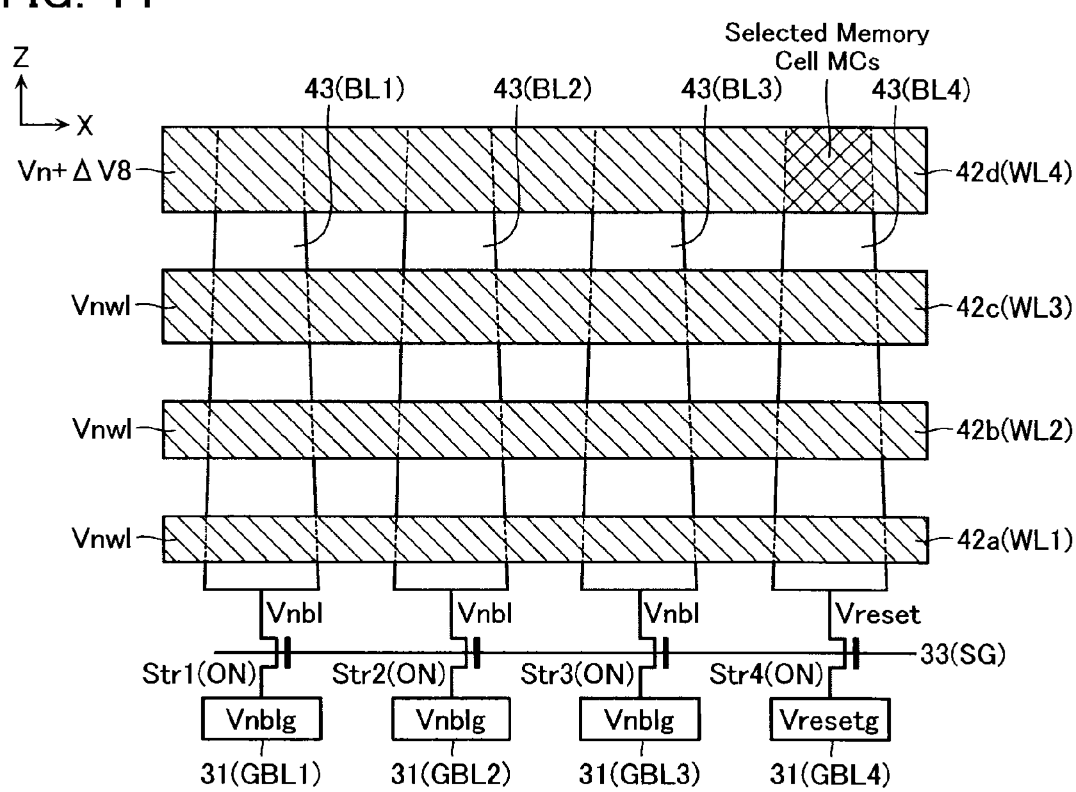
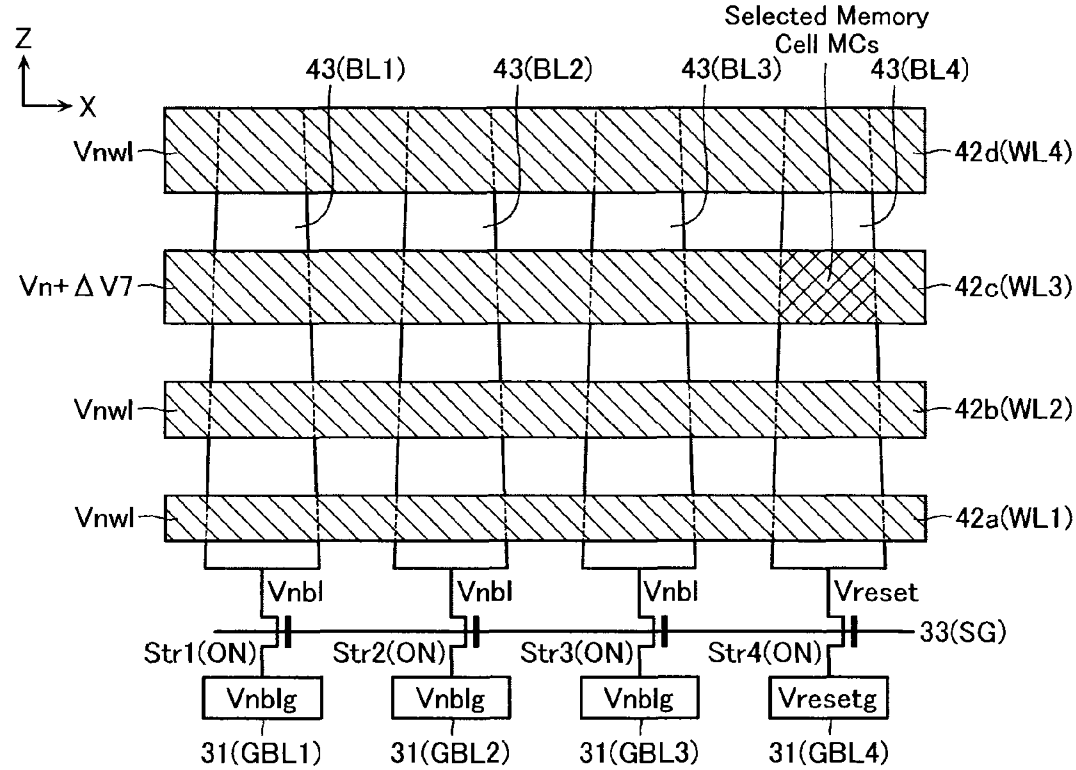
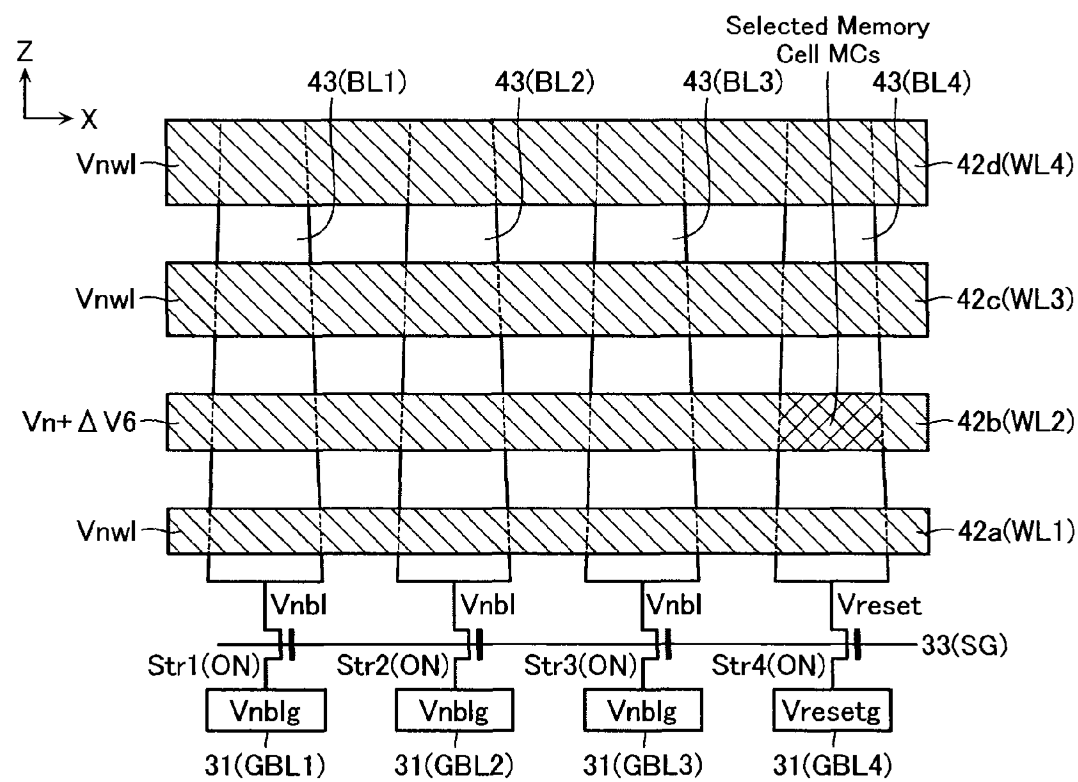

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vn+ΔV8
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 15



Z
X
Selected Memory Cell MCs
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vn+ΔV7
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 16



Z
X
Selected Memory Cell MCs
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vnwl
42c(WL3)
Vn+ΔV6
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 17

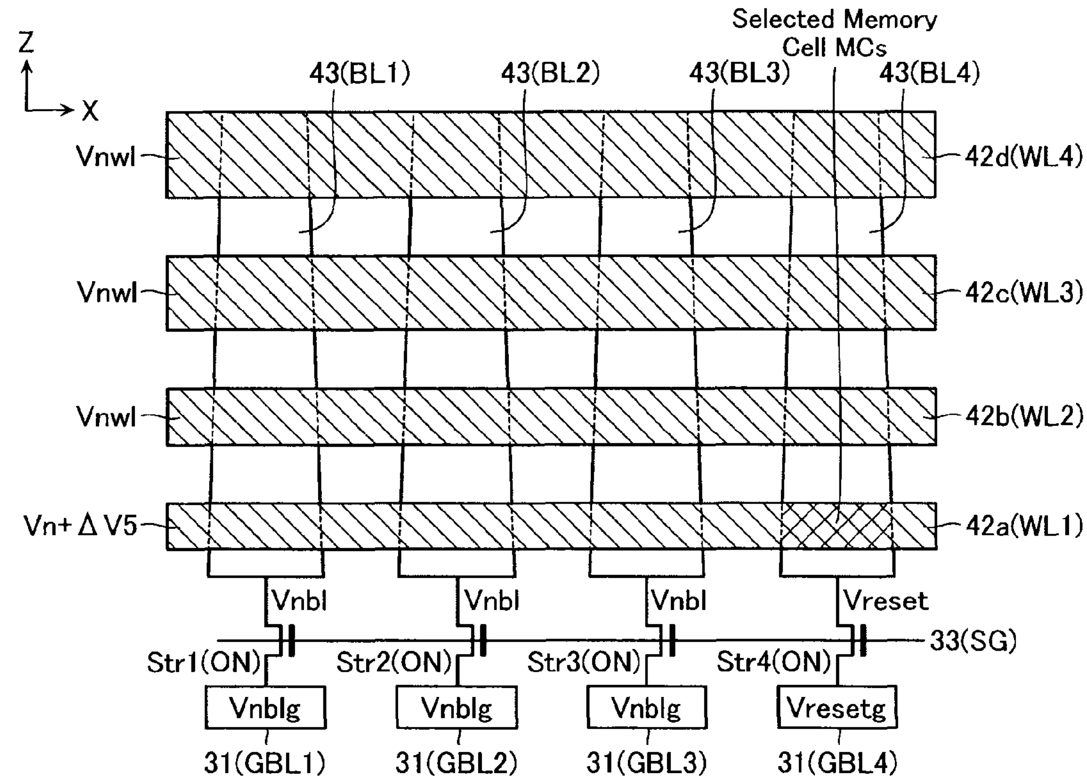


FIG. 18A

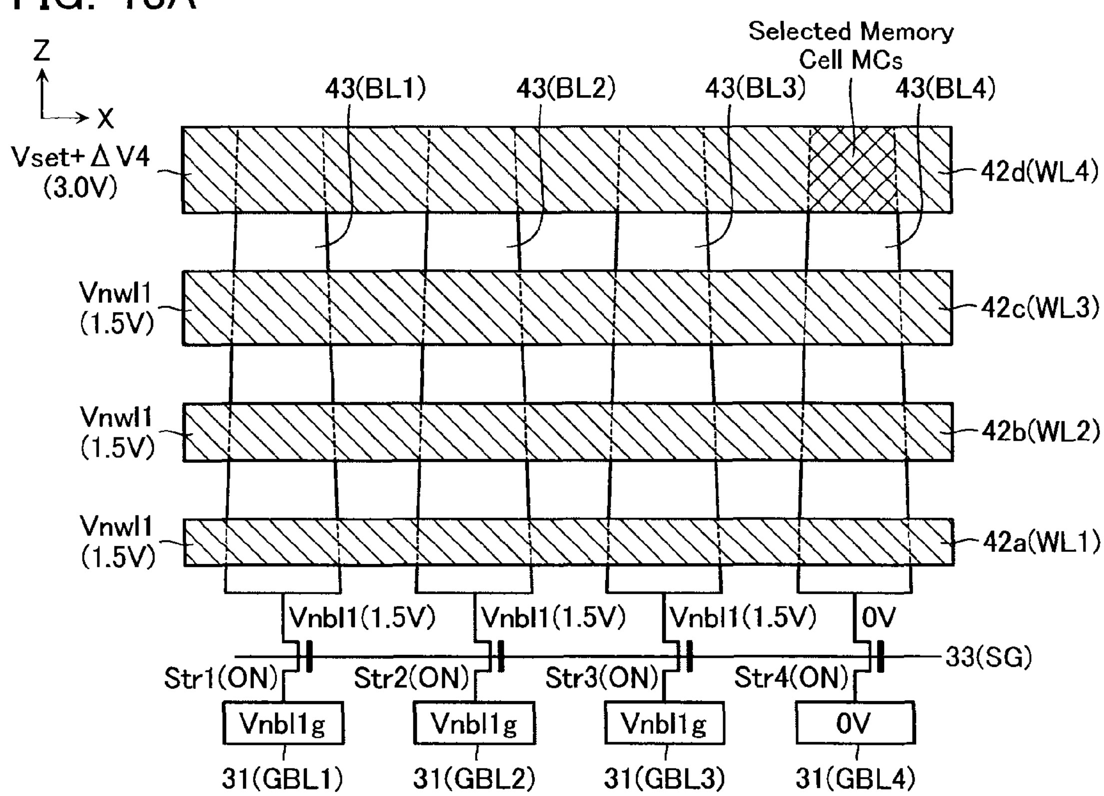


FIG. 18B

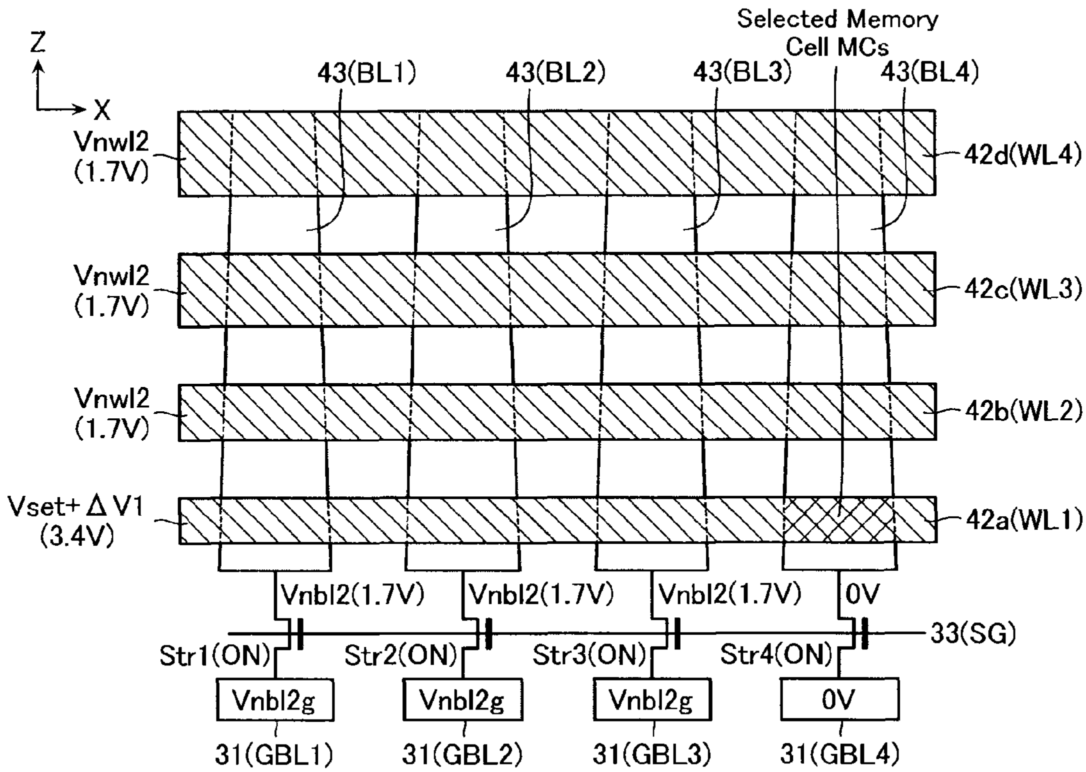


FIG. 19A

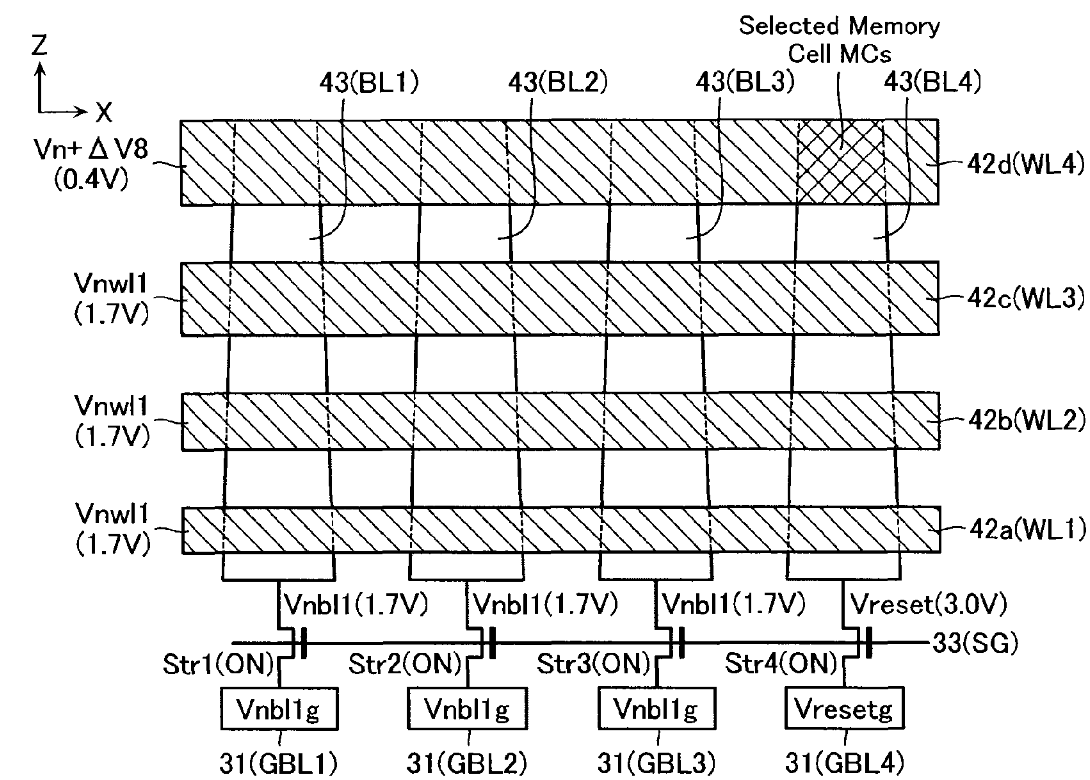


FIG. 19B

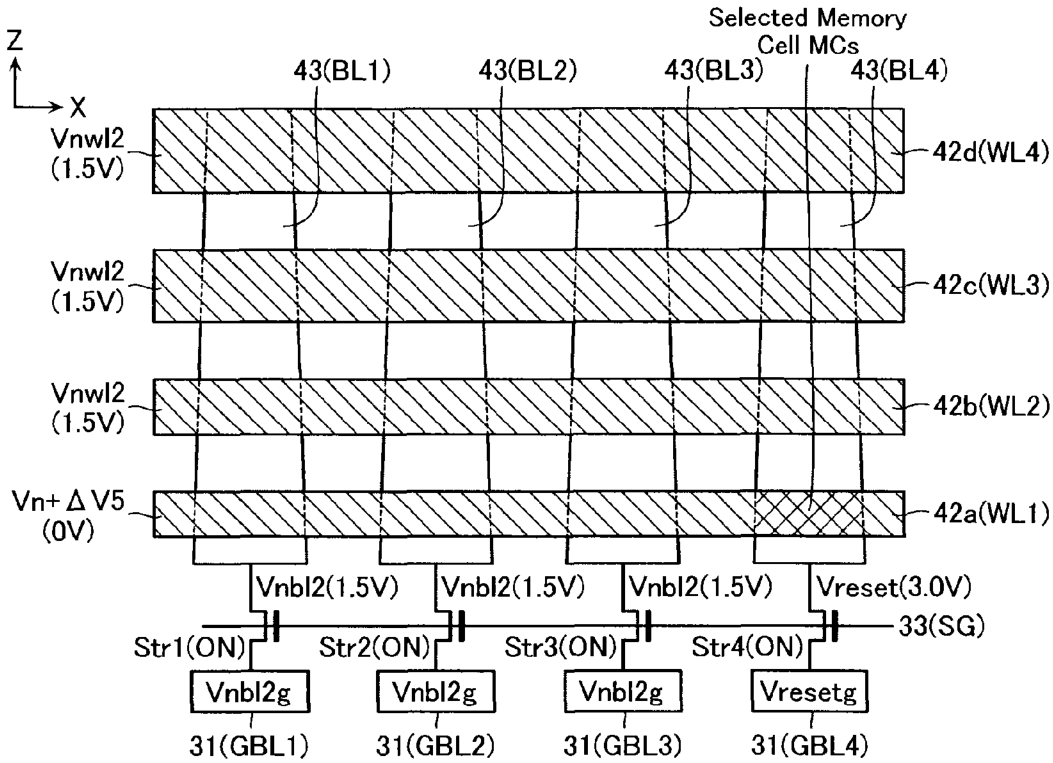


FIG. 20A

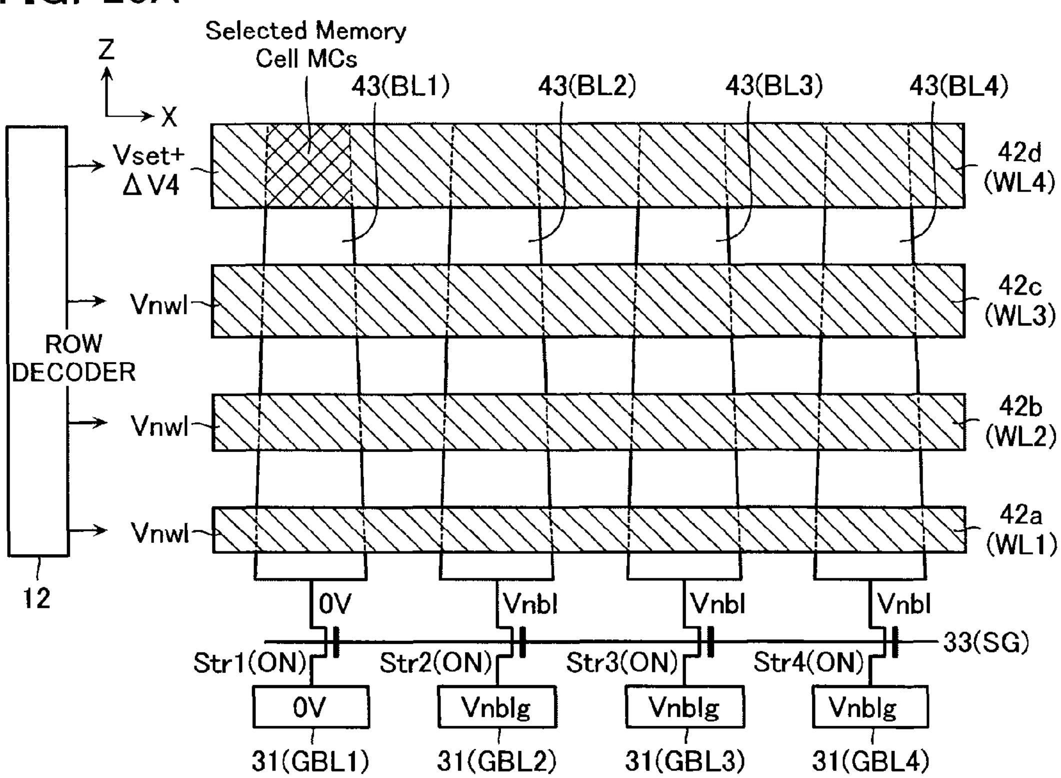


FIG. 20B

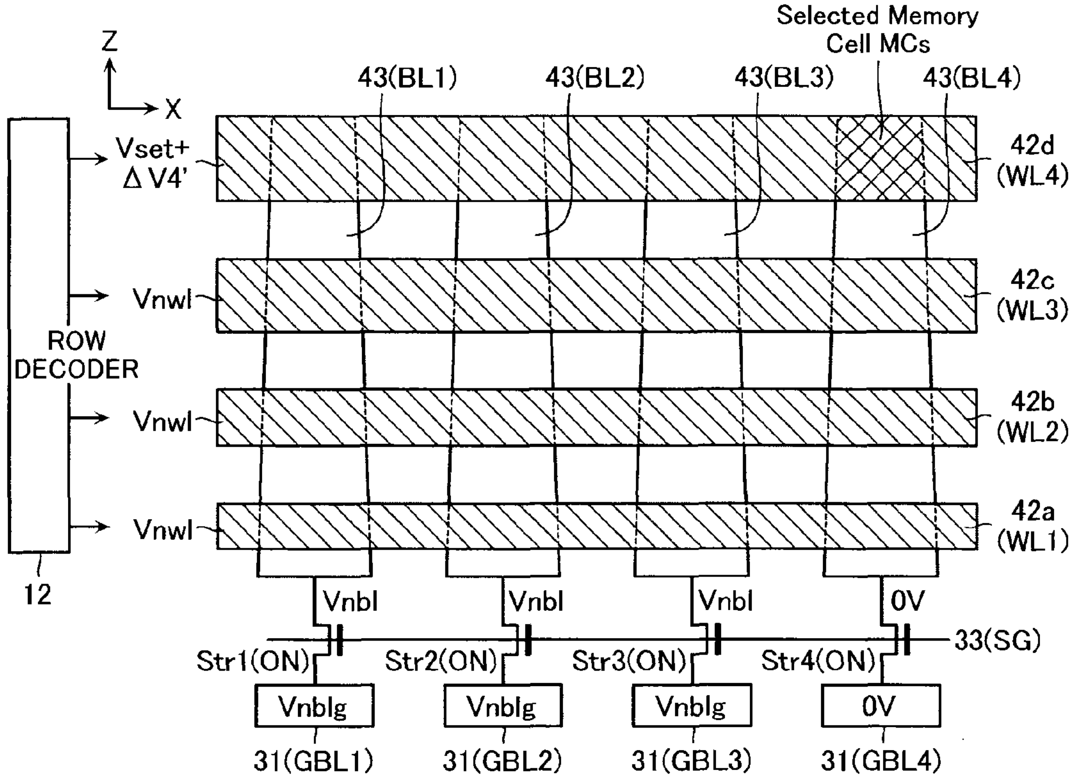


FIG. 21

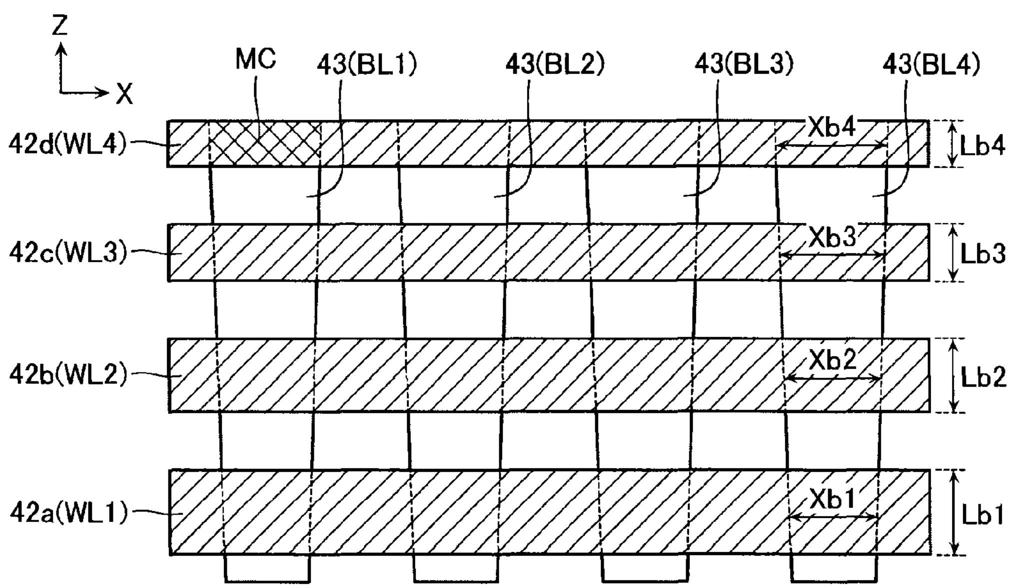
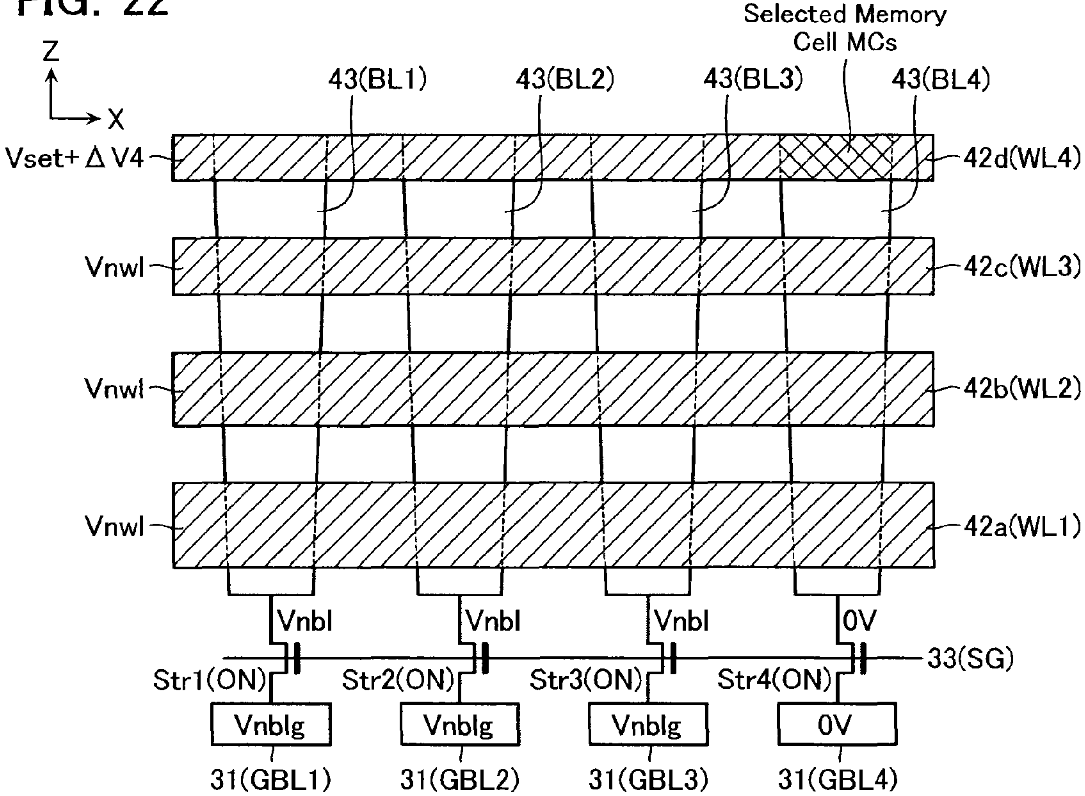
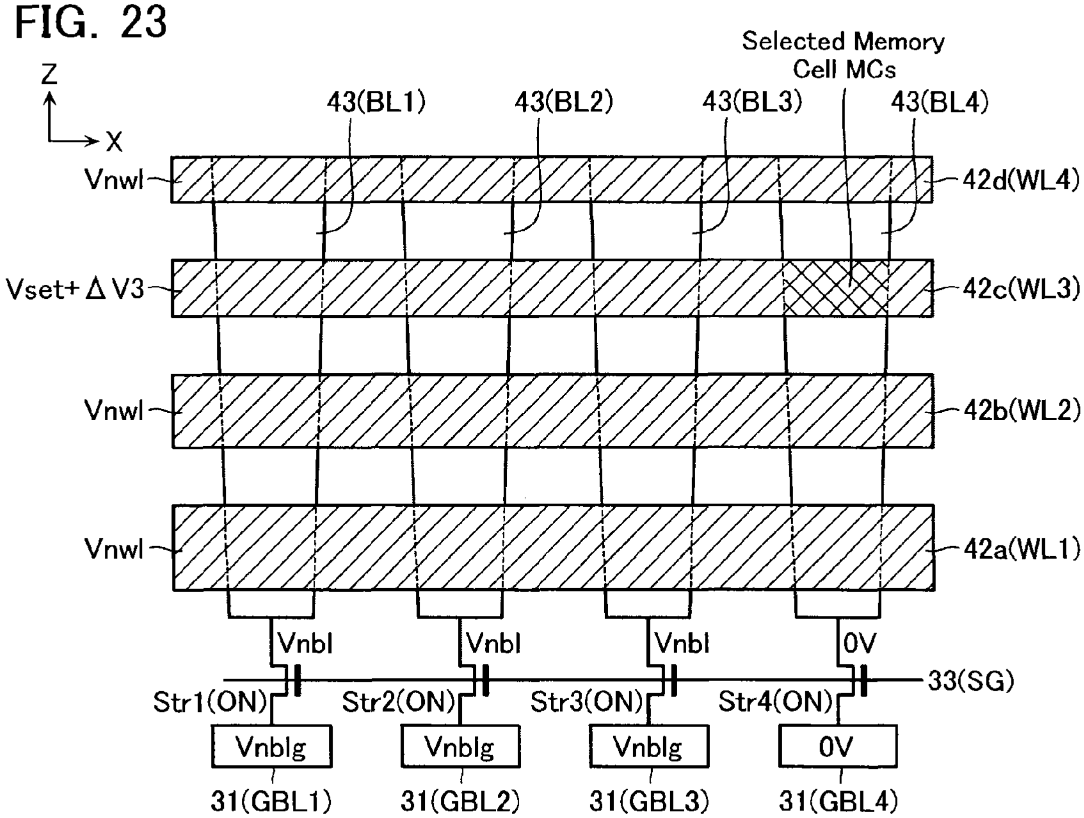


FIG. 22



Z
X
Selected Memory Cell MCs
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vset+ΔV4
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 23



Z
X
Selected Memory Cell MCs
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vset+ΔV3
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 24

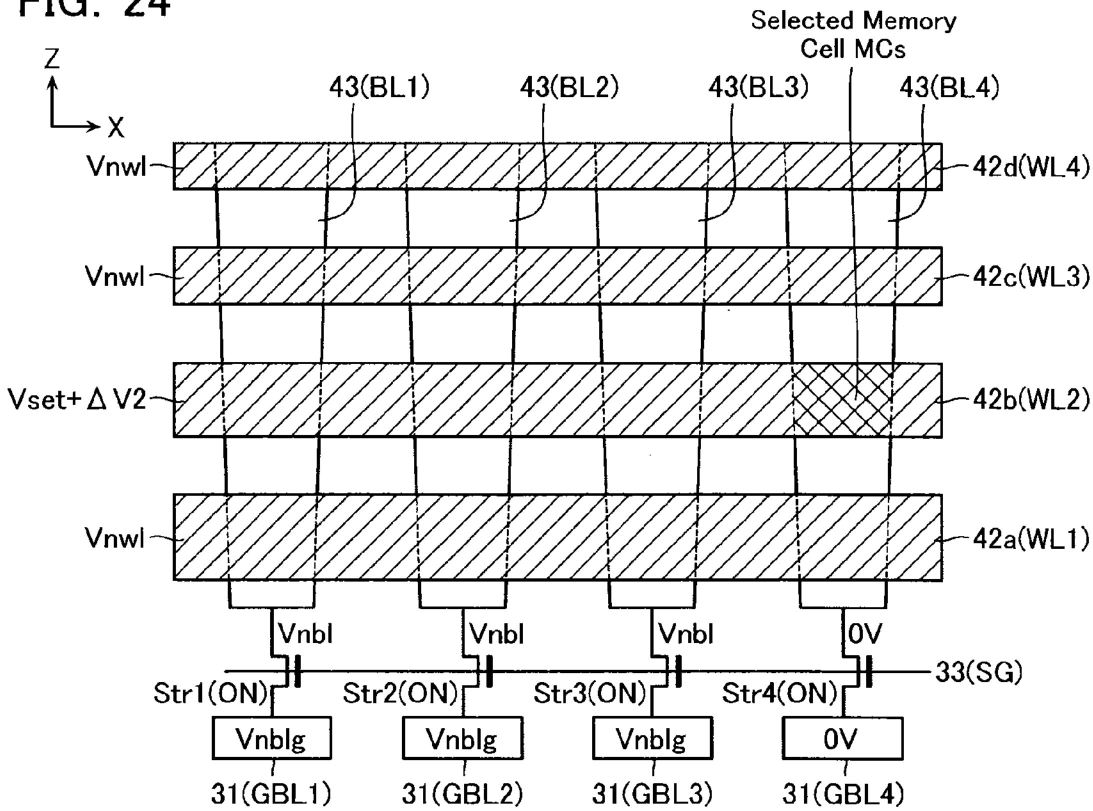

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vnwl
42c(WL3)
Vset+ΔV2
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 25

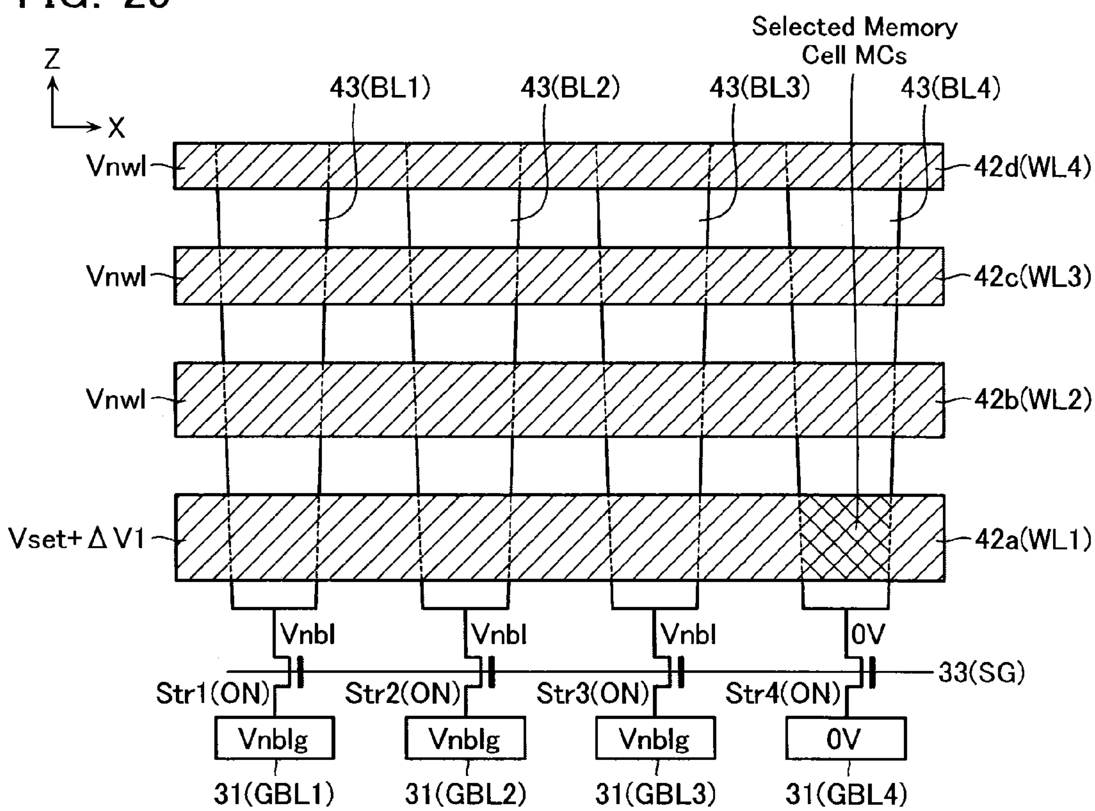
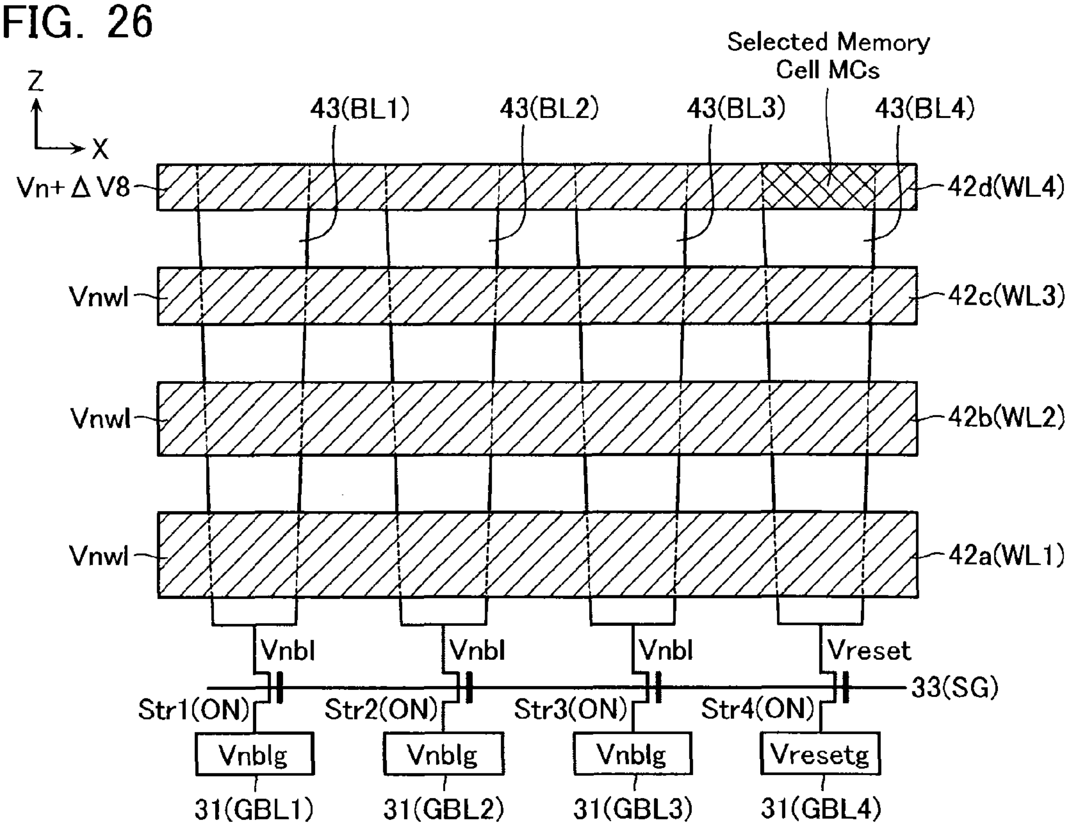
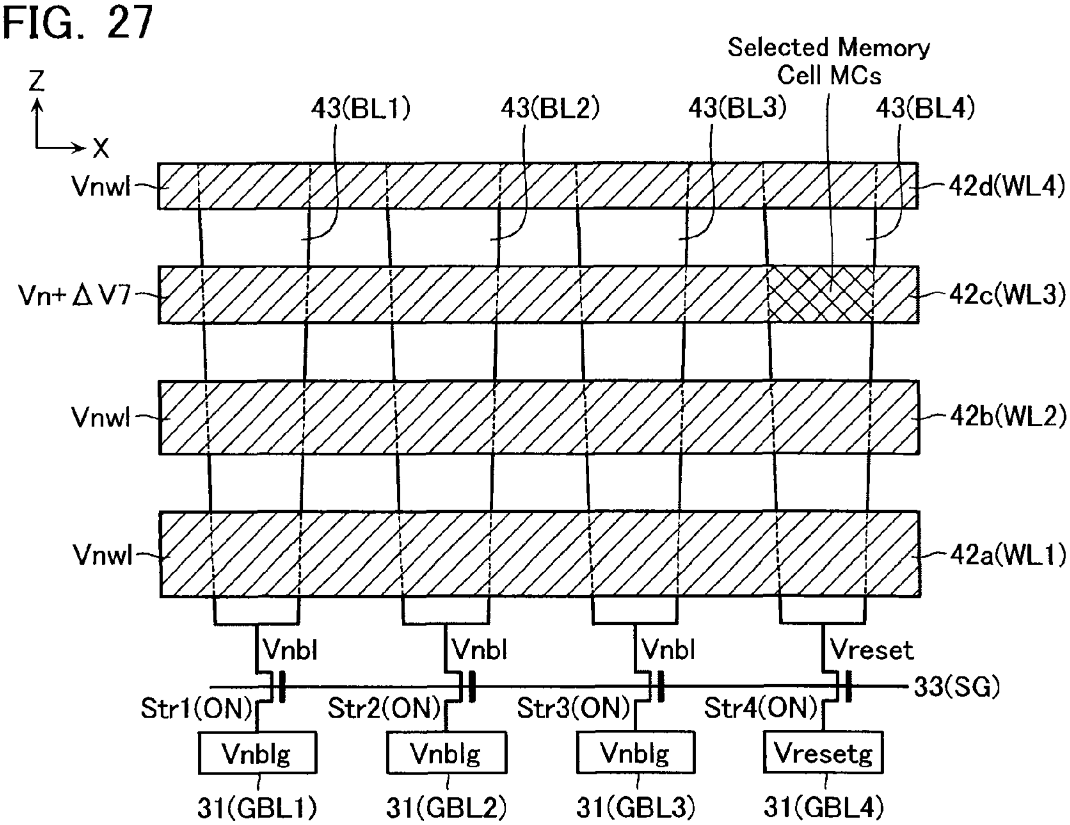

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vset+ΔV1
42a(WL1)
Vnbl
Vnbl
Vnbl
0V
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
0V
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 26



Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vn+ΔV8
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 27



Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vn+ΔV7
42c(WL3)
Vnwl
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 28

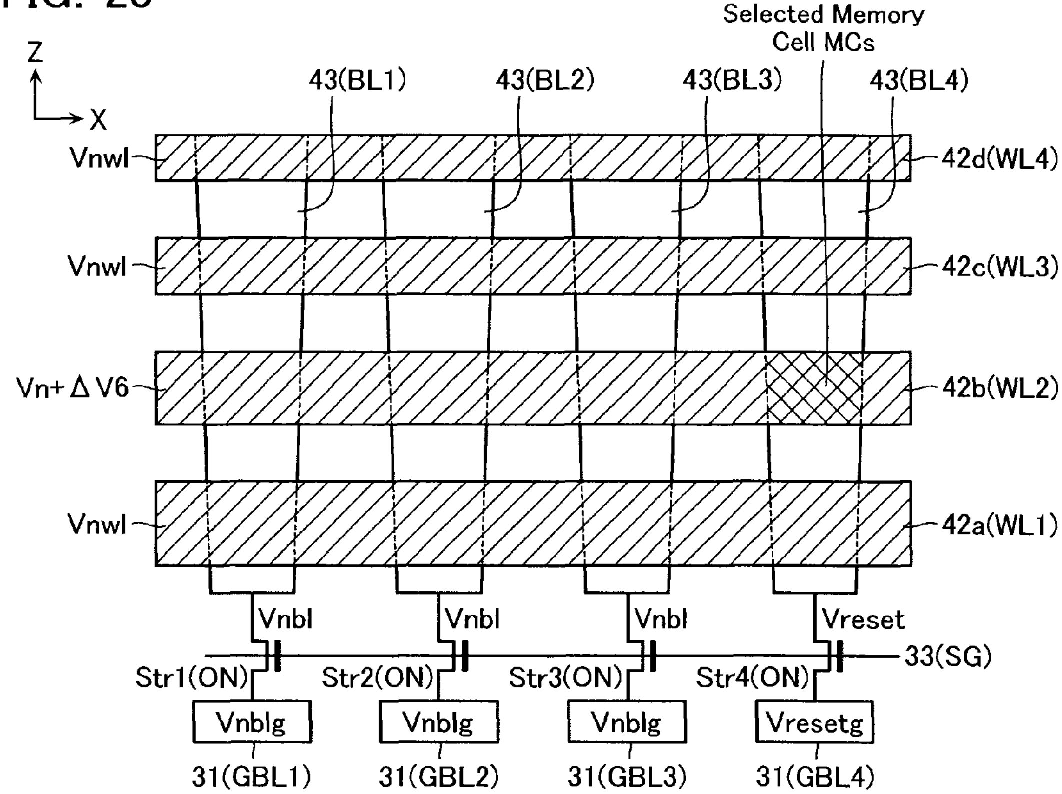

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vnwl
42c(WL3)
Vn+ΔV6
42b(WL2)
Vnwl
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 29

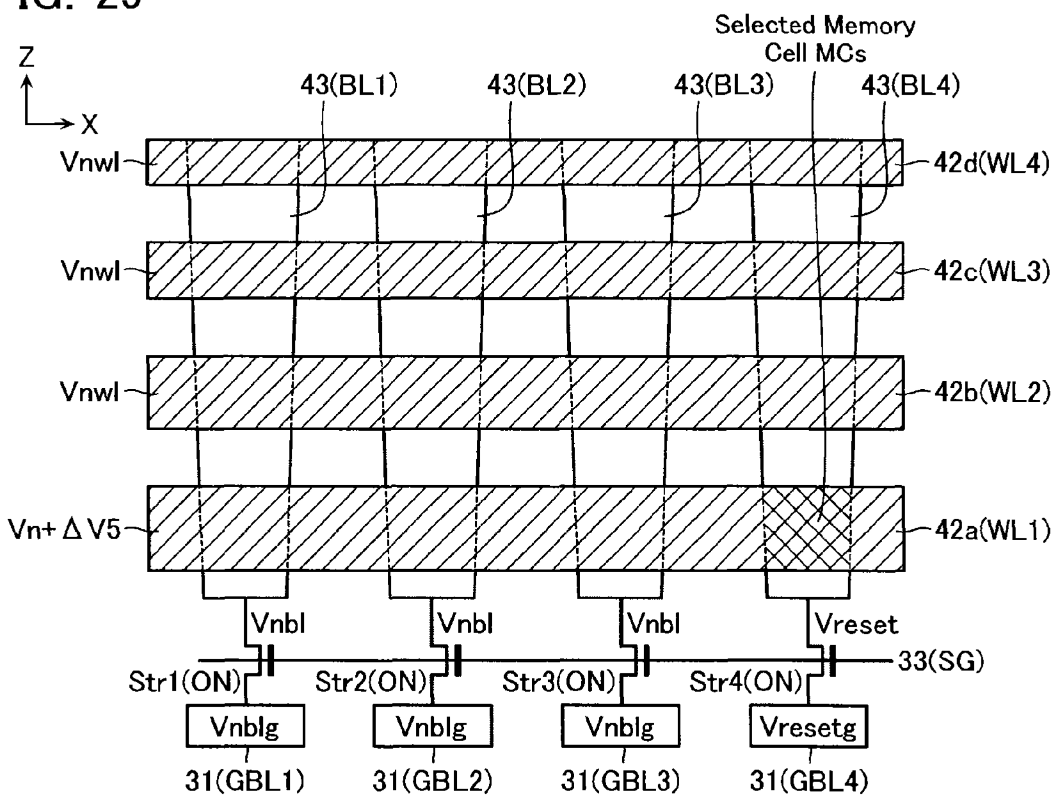

Selected Memory Cell MCs
Z
X
43(BL1)
43(BL2)
43(BL3)
43(BL4)
Vnwl
42d(WL4)
Vnwl
42c(WL3)
Vnwl
42b(WL2)
Vn+ΔV5
42a(WL1)
Vnbl
Vnbl
Vnbl
Vreset
33(SG)
Str1(ON)
Str2(ON)
Str3(ON)
Str4(ON)
Vnblg
Vnblg
Vnblg
Vresetg
31(GBL1)
31(GBL2)
31(GBL3)
31(GBL4)

FIG. 30A

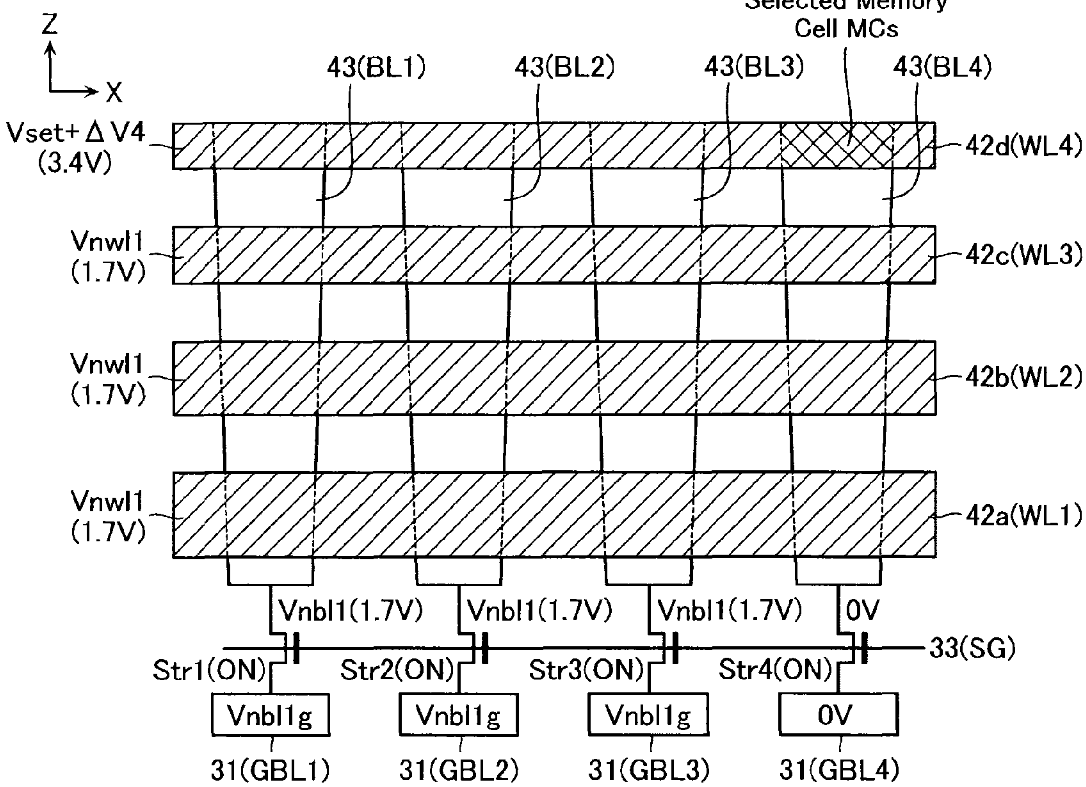


FIG. 30B

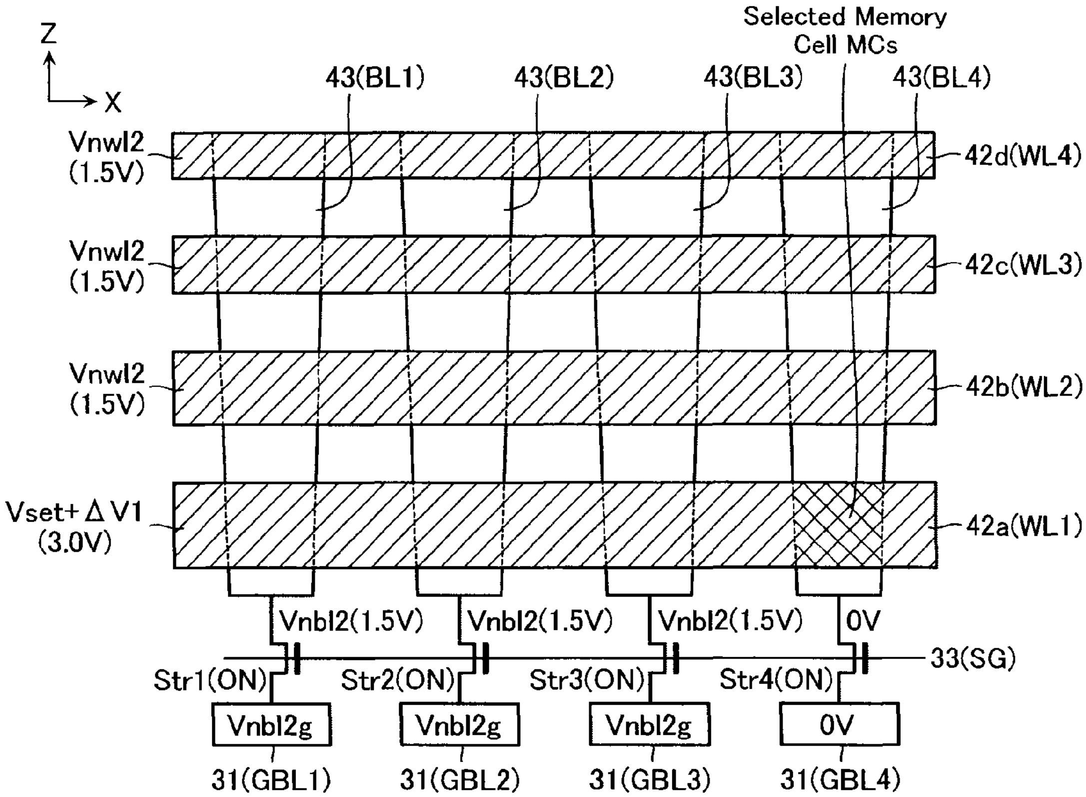


FIG. 31A

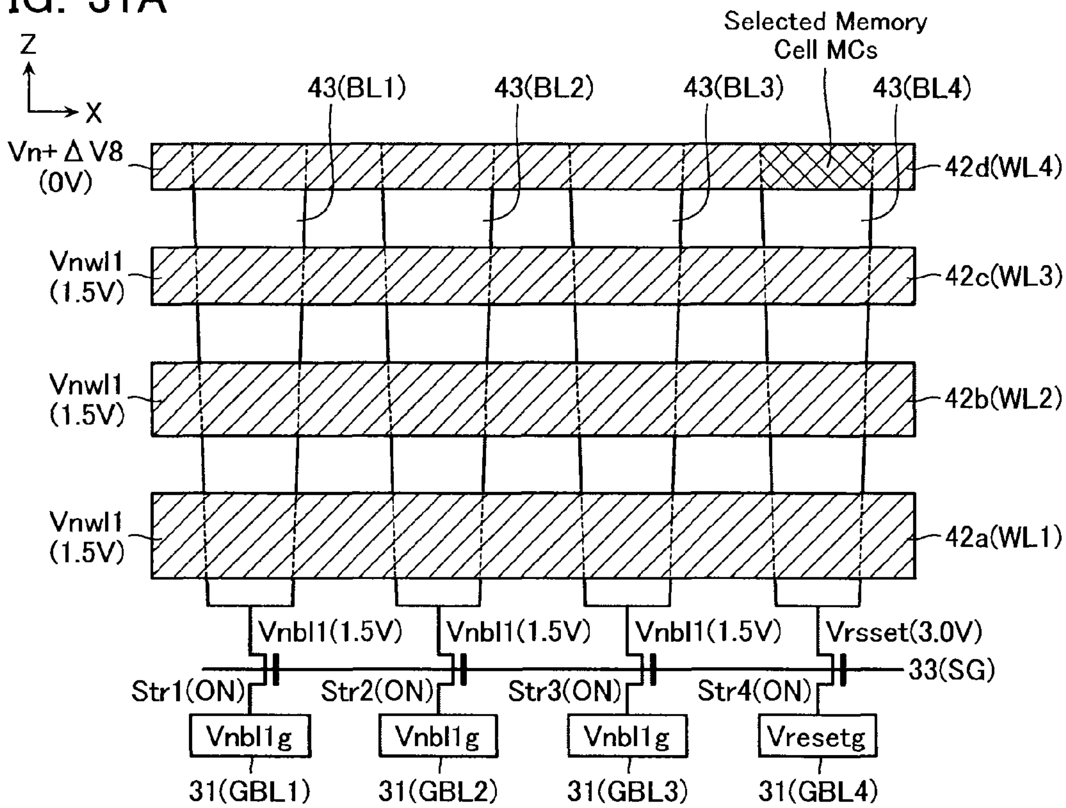


FIG. 31B

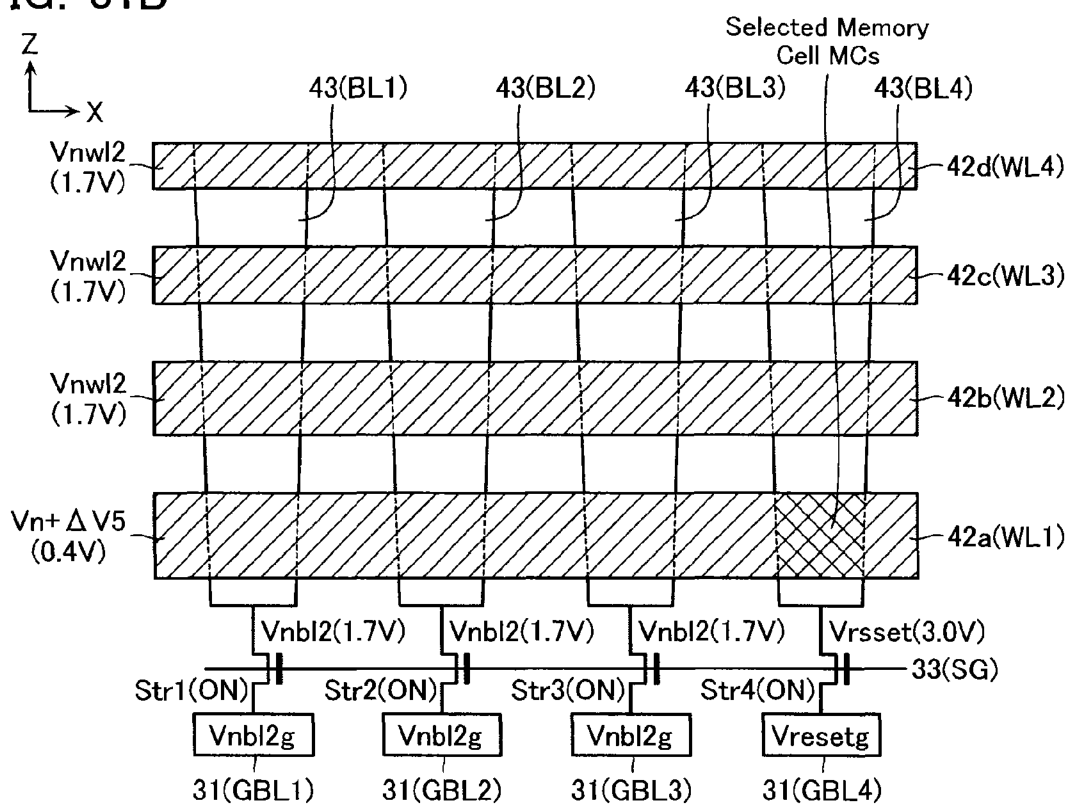


FIG. 32A

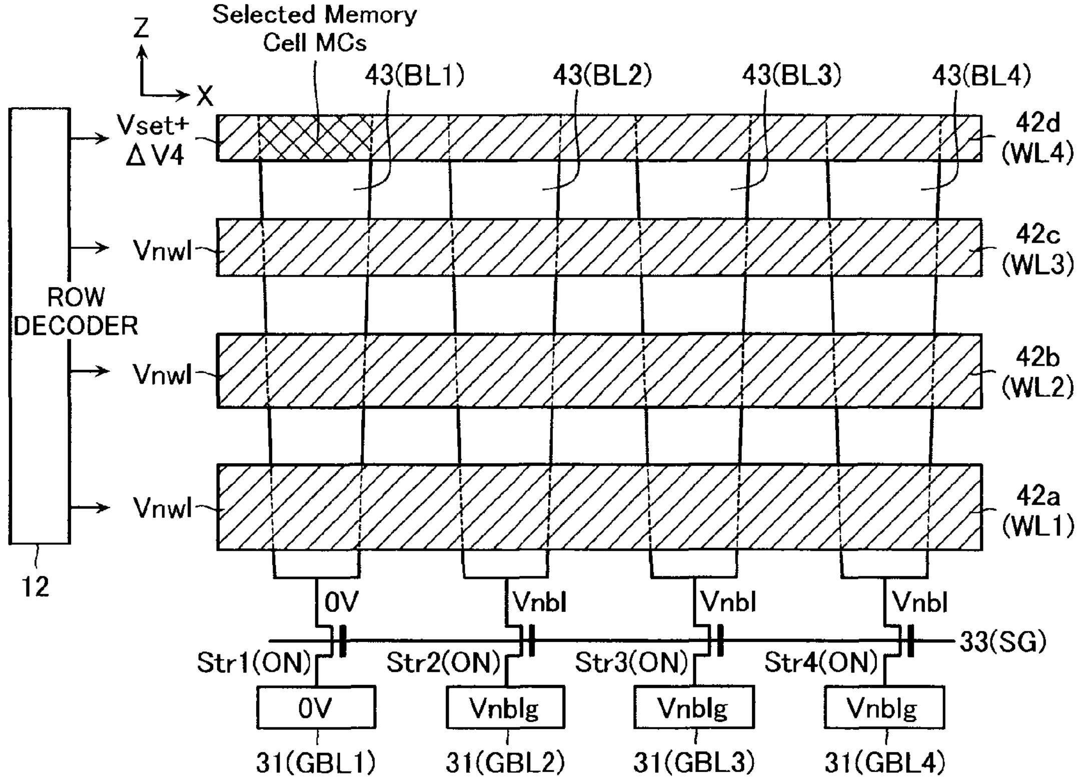
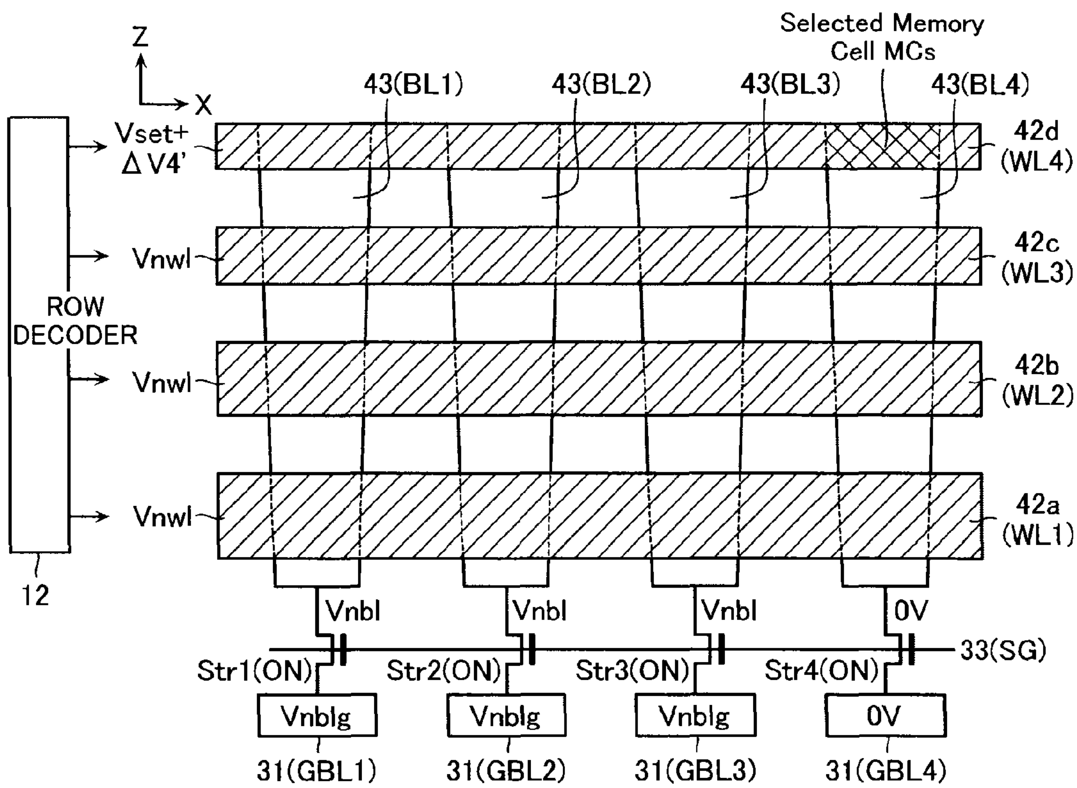


FIG. 32B



THREE-DIMENSIONAL RESISTIVE MEMORY DEVICE WITH ADJUSTABLE VOLTAGE BIASING

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of U.S. Provisional Patent Application No. 61/935,232, filed on Feb. 3, 2014, the entire contents of which are incorporated herein by reference.

BACKGROUND

1. Field

Embodiments described in the present specification relate to a semiconductor memory device.

2. Description of the Related Art

In recent years, as semiconductor memory devices have become more highly integrated, ReRAM (Resistive RAM) has been proposed. In this ReRAM, a variable resistance element that reversibly changes its resistance value is utilized as memory. Moreover, in this ReRAM, a structure where the variable resistance element is provided between a sidewall of a word line extending parallel to a principal plane of a substrate and a sidewall of a bit line extending perpendicularly to the principal plane of the substrate enables an even higher degree of integration of a memory cell array to be achieved. However, variation sometimes occurs in a voltage applied to a memory cell connected between the bit line and the word line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an example of a block diagram of a semiconductor memory device according to a first embodiment.

FIG. **2** is an example of a circuit diagram of a memory cell array **11** according to the first embodiment.

FIG. **3** is an example of a perspective view showing a stacked structure of the memory cell array **11** according to the first embodiment.

FIG. **4** is an example of a view of FIG. **3** as seen from an X direction.

FIG. **5** is an example of a top view of FIG. **3**.

FIG. **6** is an example of a view of FIG. **3** as seen from a Y direction.

FIG. **7** is an example of across-sectional view showing an outline of a method of operation of the memory cell array **11**.

FIG. **8** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the first embodiment.

FIG. **9** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the first embodiment.

FIG. **10** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the first embodiment.

FIG. **11** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the first embodiment.

FIG. **12** is an example of a cross-sectional view showing an outline of a method of operation of the memory cell array **11**.

FIG. **13** is an example of a cross-sectional view showing an outline of a method of operation of the memory cell array **11**.

FIG. **14** is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a second embodiment.

FIG. **15** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the second embodiment.

FIG. **16** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the second embodiment.

FIG. **17** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the second embodiment.

FIG. **18**A is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a third embodiment.

FIG. **18**B is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the third embodiment.

FIG. **19**A is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a fourth embodiment.

FIG. **19**B is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the fourth embodiment.

FIG. **20**A is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a fifth embodiment.

FIG. **20**B is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the fifth embodiment.

FIG. **21** is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a sixth embodiment.

FIG. **22** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the sixth embodiment.

FIG. **23** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the sixth embodiment.

FIG. **24** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the sixth embodiment.

FIG. **25** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the sixth embodiment.

FIG. **26** is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a seventh embodiment.

FIG. **27** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the seventh embodiment.

FIG. **28** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the seventh embodiment.

FIG. **29** is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the seventh embodiment.

FIG. **30**A is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to an eighth embodiment.

FIG. **30**B is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the eighth embodiment.

FIG. **31**A is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a ninth embodiment.

FIG. **31**B is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the ninth embodiment.

FIG. **32**A is an example of a cross-sectional view showing a method of operation of a memory cell array **11** according to a tenth embodiment.

FIG. **32**B is an example of a cross-sectional view showing a method of operation of the memory cell array **11** according to the tenth embodiment.

DETAILED DESCRIPTION

A semiconductor memory device according to an embodiment comprises a memory cell array and a control circuit. The memory cell array includes: a plurality of first conductive layers that are stacked in a first direction perpendicular to a substrate and extend in a second direction parallel to the substrate; a memory layer provided on a side surface of the plurality of the first conductive layers; and a second conductive layer that extends in the first direction and includes a first side surface that contacts the side surface of the plurality of the first conductive layers via the memory layer. A width in the second direction of the first side surface of the second conductive layer at a first position in the first direction is smaller than a width in the second direction of the first side surface of the second conductive layer at a second position lower than the first position. A thickness in the first direction of the first conductive layer disposed at the first position is larger than a thickness in the first direction of the first conductive layer disposed at the second position. The control circuit is configured to apply a first voltage to a selected first conductive layer of the first conductive layers and provide a second voltage to the second conductive layer. The control circuit is configured capable of, when the control circuit applies the first voltage to the selected first conductive layer, changing a value of the first voltage based on a position in the first direction of the selected first conductive layer.

First Embodiment

[Configuration]

First, an overall configuration of a semiconductor memory device according to a first embodiment will be described. FIG. **1** is an example of a block diagram of the semiconductor memory device according to the first embodiment. As shown in FIG. **1**, a semiconductor memory device **1** includes a memory cell array **11**, a row decoder **12**, a column decoder **13**, a higher-level block **14**, a power supply **15**, and a control circuit **16**.

The memory cell array **11** includes a plurality of word lines WL and bit lines BL that intersect each other, and memory cells MC disposed one at each of intersections of these word lines WL and bit lines BL. The row decoder **12** selects the word line WL during access (data erase/write/read). The column decoder **13** selects the bit line BL during access, and includes a driver that controls an access operation.

The higher-level block **14** selects the memory cell MC which is to be an access target in the memory cell array **11**. The higher-level block **14** provides a row address and a column address to, respectively, the row decoder **12** and the column decoder **13**. The power supply **15** generates certain combinations of voltages corresponding to each of operations of data erase/write/read, and supplies these combinations of voltages to the row decoder **12** and the column decoder **13**. The control circuit **16** performs control of, for example, sending the addresses to the higher-level block **14**, and, moreover, performs control of the power supply **15**, based on a command from a host or memory controller **20**.

Next, the memory cell array **11** according to the first embodiment will be described in detail with reference to FIGS. **2** and **3**. FIG. **2** is an example of a circuit diagram of the memory cell array **11**. FIG. **3** is an example of a perspective view showing a stacked structure of the memory cell array **11**. Note that in FIG. **2**, an X direction, a Y direction, and a Z direction are orthogonal to each other, and the X direction is a direction perpendicular to a plane of paper. In addition, a structure shown in FIG. **2** is provided repeatedly in the X direction.

As shown in FIG. **2**, the memory cell array **11** includes a select transistor STr, a global bit line GBL, and a select gate line SG, in addition to the above-mentioned word line WL, bit line BL, and memory cell MC.

As shown in FIGS. **2** and **3**, word lines WL**1** to WL**4** are arranged in the Z direction with a certain pitch, and extend in the X direction. The bit lines BL are arranged in a matrix in the X direction and the Y direction, and extend in the Z direction. The memory cells MC are disposed at places where these word lines WL and bit lines BL intersect. Therefore, the memory cells MC are arranged in a three-dimensional matrix in the X, Y, and Z directions. In various kinds of operations, a selected word line WL of the word lines WL**1** to WL**4** can have any voltage applied thereto. In addition, a non-selected word line WL of the word lines WL**1** to WL**4** can have any voltage applied thereto.

As shown in FIG. **2**, the memory cell MC includes a variable resistance element VR. The variable resistance element VR is electrically rewritable and can store data based on a resistance value of the variable resistance element VR. The variable resistance element VR changes from a high-resistance state (reset state) to a low-resistance state (set state) by a setting operation that applies a certain voltage or more to both terminals of the variable resistance element VR, and changes from the low-resistance state (set state) to the high-resistance state (reset state) by a resetting operation that applies a certain voltage or more to both terminals of the variable resistance element VR. Moreover, a resistance state of the variable resistance element VR is read by a read operation that applies a certain voltage or more to both terminals of the variable resistance element VR.

In addition, the variable resistance element VR, immediately after manufacturing, is in a state where its resistance state cannot be easily changed, and is in a high-resistance state. Accordingly, a forming operation is executed. In the forming operation, a high voltage greater than or equal to that of the setting operation and the resetting operation is applied to both terminals of the variable resistance element VR. As a result of this forming operation, a region (filament path) where locally it is easy for a current to flow is formed in the variable resistance element VR, whereby the variable resistance element VR can have its resistance state changed easily, and achieves a state of being operable as a storage element.

As shown in FIG. **2**, the select transistor STr is provided between the global bit line GBL and one end of the bit line BL. The global bit lines GBL are aligned with a certain pitch in the X direction, and extend in the Y direction. One global bit line GBL is commonly connected to one ends of a plurality of select transistors STr arranged in a line in the Y direction. In addition, electrodes disposed between two select transistors STr arranged adjacently in the Y direction are commonly connected. The select gate lines SG are aligned with a certain pitch in the Y direction, and extend in the X direction. One select gate line SG is commonly connected to gates of a plurality of the select transistors STr arranged in a line in the X direction. Note that it is also possible to separate gate electrodes of two select transistors STr arranged adjacently in the Y direction and thereby operate each of the two select transistors STr independently.

Next, a stacked structure of the memory cell array **11** according to the first embodiment will be described with reference to FIGS. **3**, **4**, and **5**. FIG. **4** is a view of an F**4**-F**4** plane of FIG. **3** as seen from the X direction (Z-Y plane view), and FIG. **5** is a top view of FIG. **3**. Note that in FIGS. **3** and **5**, an interlayer insulating film is omitted.

As shown in FIGS. **3** and **4**, the memory cell array **11** includes a select transistor layer **30** and a memory layer **40** that are stacked on a substrate **20**. The select transistor layer **30** functions as the select transistor STr, and the memory layer **40** functions as the memory cell MC.

As shown in FIGS. **3** and **4**, the select transistor layer **30** includes a conductive layer **31**, an interlayer insulating layer **32**, a conductive layer **33**, and an interlayer insulating layer **34**. These conductive layer **31**, interlayer insulating layer **32**, conductive layer **33**, and interlayer insulating layer **34** are stacked in the Z direction perpendicular to the substrate **20**. The conductive layer **31** functions as the global bit line GBL, and the conductive layer **33** functions as the select gate line SG and as the gate of the select transistor STr.

The conductive layers **31** are aligned with a certain pitch in the X direction parallel to the substrate **20**, and extend in the Y direction (refer to FIG. **5**). The interlayer insulating layer **32** covers an upper surface of the conductive layer **31**. The conductive layers **33** are aligned with a certain pitch in the Y direction, and extend in the X direction (refer to FIG. **5**). The interlayer insulating layer **34** covers a side surface and an upper surface of the conductive layer **33**. For example, the conductive layers **31** and **33** are configured by polysilicon. The interlayer insulating layers **32** and **34** are configured by silicon oxide (SiO_2).

In addition, as shown in FIGS. **3** and **4**, the select transistor layer **30** includes, for example, a column-shaped semiconductor layer **35** and a gate insulating layer **36**. The semiconductor layer **35** functions as a body (channel) of the select transistor STr, and the gate insulating layer **36** functions as a gate insulating film of the select transistor STr.

The semiconductor layers **35** are disposed in a matrix in the X and Y directions, and extend in a column shape in the Z direction. In addition, the semiconductor layer **35** contacts the upper surface of the conductive layer **31**, and contacts a side surface in the Y direction of the conductive layer **33** via the gate insulating layer **36**. Moreover, the semiconductor layer **35** includes an N+ type semiconductor layer **35***a*, a P− type semiconductor layer **35***b*, and an N+ type semiconductor layer **35***c* that are stacked.

As shown in FIGS. **3** and **4**, the N+ type semiconductor layer **35***a* contacts the interlayer insulating layer **32** at a side surface in the Y direction of the N+ type semiconductor layer **35***a*. The P− type semiconductor layer **35***b* contacts a side surface of the conductive layer **33** at a side surface in the Y direction of the P− type semiconductor layer **35***b*. The N+ type semiconductor layer **35***c* contacts the interlayer insulating layer **34** at a side surface in the Y direction of the N+ type semiconductor layer **35***c*. The N+ type semiconductor layers **35***a* and **35***c* are configured by polysilicon implanted with an N type impurity at a high concentration (for example, 1×10^{19} to 1×10^{21} cm^{-3}), and the P− type semiconductor layer **35***b* is configured by polysilicon implanted with a P type impurity at a low concentration (for example, 1×10^{15} to 1×10^{19} cm^{-3}). The gate insulating layer **36** is configured by, for example, silicon oxide (SiO_2).

As shown in FIGS. **3** and **4**, the memory layer **40** includes, stacked alternately in the Z direction, interlayer insulating layers **41***a* to **41***d* and conductive layers **42***a* to **42***d*. The conductive layers **42***a* to **42***d* function as the word lines WL**1** to WL**4**, respectively. The conductive layers **42***a* to **42***d*, when viewed from the Z direction, each include a pair of comb tooth shapes facing each other in the X direction (refer to FIG. **5**). The interlayer insulating layers **41***a* to **41***d* are configured by, for example, silicon oxide (SiO_2), and the conductive layers **42***a* to **42***d* are configured by, for example, polysilicon.

Moreover, as shown in FIG. **4**, the higher a layer in which a certain one of the conductive layers **42***a* to **42***d* is positioned, the larger is a thickness in the Z direction of that conductive layer. That is, a thickness La**4** in the Z direction of the conductive layer **42***d* is larger than a thickness La**3** in the Z direction of the conductive layer **42***c* in a layer below the conductive layer **42***d*. Similarly, the thickness La**3** in the Z direction of the conductive layer **42***c* is larger than a thickness La**2** in the Z direction of the conductive layer **42***b* in a layer below the conductive layer **42***c*, and the thickness La**2** in the Z direction of the conductive layer **42***b* is larger than a thickness La**1** in the Z direction of the conductive layer **42***a* in a layer below the conductive layer **42***b*. Now, a film thickness of the conductive layers **42***a* to **42***d* could be said to become gradually larger in the Z direction.

In addition, as shown in FIGS. **3** and **4**, the memory layer **40** includes, for example, a column-shaped conductive layer **43** and a variable resistance layer **44**. The conductive layer **43** functions as the bit line BL. The variable resistance layer **44** functions as the variable resistance element VR.

The conductive layers **43** are disposed in a matrix in the X and Y directions, contact an upper surface of the semiconductor layer **35**, and extend in a column shape in the Z direction. The variable resistance layer **44** is provided between a side surface in the Y direction of the conductive layer **43** and side surfaces in the Y direction of the interlayer insulating layers **41***a* to **41***d*. In addition, the variable resistance layer **44** is provided between the side surface in the Y direction of the conductive layer **43** and side surfaces in the Y direction of the conductive layers **42***a* to **42***d*. The conductive layer **43** is configured by, for example, polysilicon. The variable resistance layer **44** is composed mainly of an oxide including at least any one element selected from the group consisting of Hf, Zr, Ni, Ta, W, Co, Al, Fe, Mn, Cr, and Nb. The variable resistance layer **44** is configured by, for example, a metal oxide (for example, HfO_2, Al_2O_3, TiO_2, NiO, WO_3, Ta_2O_5, and so on).

In addition, the variable resistance layer **44** may employ Si in a polycrystalline or amorphous state, or SiO, SiON, SiN, Ge, SiGe, GaAs, InP, GaP, GaInAsP, GaN, SiC, HfSiO, HfO, AlO, and so on. Moreover, a stacked film of the above-mentioned materials may also be employed in the variable resistance layer **44**. Furthermore, the following may be disposed in the conductive layer **43** or the conductive layers **42***a* to **42***d* as an electrode of a resistance varying material, namely an electrode of, for example, Ag, Au, Ti, Ni, Co, Al, Fe, Cr, Cu, W, Hf, Ta, Pt, Ru, Zr, or Ir, or a nitride or carbide of these, and so on. In addition, a material having the above-described materials added to polycrystalline silicon may also be employed as the electrode. Moreover, a stopper layer of TaSiN may also be inserted on an opposite side to the electrode of the variable resistance layer **44**.

Next, a shape of the conductive layer **43** and the conductive layers **42***a* to **42***d* will be described specifically, with reference to FIG. **6**. FIG. **6** is a view of an F**6**-F**6** plane of FIG. **3** as seen from the Y direction (Z-X plane view). Note that in FIG. **6**, the interlayer insulating layers **41***a* to **41***d* and the variable resistance layer **44** are omitted.

As shown in FIG. **6**, the conductive layer **43** is formed in a tapered shape as seen from the Y direction, and a width in the X direction of a side surface in the Y direction of the conductive layer **43** becomes gradually smaller proceeding in a +Z direction (upward direction of FIG. **6**). That is, the width in the X direction of the side surface in the Y direction of the conductive layer **43** at a first position is smaller than the width in the X direction of the side surface in the Y direction of the conductive layer **43** at a second position lower than the first position. For example, as shown in FIG. **6**, if a width of the conductive layer **43** at a position corresponding to the conductive layer **42***a* is assumed to be Xa**1**, a width of the conductive layer **43** at a position corresponding to the conductive layer **42***b* is assumed to be Xa**2**, a width of the conductive layer **43** at a position corresponding to the conductive layer **42***c* is assumed to be Xa**3**, and a width of the conductive layer **43** at a position corresponding to the conductive layer **42***d* is assumed to be Xa**4**, then Xa**1**>Xa**2**>Xa**3**>Xa**4**. Note that this tapered shape of the conductive layer **43** can be formed by adjusting an etching condition during manufacturing. As mentioned above, in the present embodiment, the higher a layer in which a certain one of the conductive layers **42***a* to **42***d* is positioned, the larger a thickness in the Z direction of that conductive layer is made. Now, if thicknesses in the Z direction of the conductive layers **42***a* to **42***d* are assumed to be substantially uniform, then a facing area between the conductive layer **42***a* and the conductive layer **43** is largest, and a facing area between the conductive layer **42***d* and the conductive layer **43** is smallest. As a result, variation occurs in characteristics of the variable resistance element VR formed between the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) and the conductive layer **43** (bit line BL).

Accordingly, in the present embodiment, as shown in FIG. **6**, the higher a layer in which the conductive layers **42***a* to **42***d* are positioned, the larger the thicknesses La**1** to La**4** in the Z direction are made in accordance with the above-described shape of the conductive layer **43**. For example, as shown in FIG. **6**, if the thickness of the conductive layer **42***a* is assumed to be La**1**, the thickness of the conductive layer **42***b* is assumed to be La**2**, the thickness of the conductive layer **42***c* is assumed to be La**3**, and the thickness of the conductive layer **42***d* is assumed to be La**4**, then La**1**<La**2**<La**3**<La**4**. Therefore, facing areas between the conductive layers **42***a* to **42***d* and the conductive layer **43** can be made substantially constant. As a result, in the present embodiment, variation in characteristics of the variable resistance element VR can be suppressed.

[Method of Operation]

First, an outline of the setting operation will be described with reference to FIG. **7**, and then a method of an operation of the semiconductor memory device according to the present embodiment will be described with reference to FIGS. **8** to **11**.

FIG. **7** is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC.

In the present embodiment, it is assumed that the setting operation is executed on a selected memory cell MCs provided between the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**). In this case, the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**) become, respectively, a selected word line WL and a selected bit line BL. Moreover, the conductive layers **42***a* to **42***c* (word lines WL**1** to WL**3**) and the conductive layers **43** (bit lines BL**1** to BL**3**) become, respectively, non-selected word lines WL and non-selected bit lines BL.

The setting operation is executed by applying to the selected memory cell MCs a setting voltage such that the variable resistance element VR changes from the high-resistance state (reset state) to the low-resistance state (set state). During the setting operation, the control circuit **16** applies a setting voltage Vset to the conductive layer **42***d* (selected word line WL**4**), and keeps a voltage of the conductive layer (selected global bit line GBL**4**) connected to the conductive layer **43** (selected bit line BL**4**) at 0 V.

During the setting operation, the control circuit **16** applies a non-selected word line voltage Vnwl to the conductive layers **42***a* to **42***c* (non-selected word lines WL**1** to WL**3**), and applies a non-selected global bit line voltage Vnblg to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Now, the control circuit **16** sets the select transistors STr**1** to STr**4** to an on state. Due to this, 0 V is transferred to the conductive layer **43** (selected bit line BL**4**), and a non-selected bit line voltage Vnbl slightly lower than the non-selected global bit line voltage Vnblg is transferred to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). As a result, the setting operation can be executed on the selected memory cell MCs only. Moreover, the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl are set to a voltage such that the setting operation is not mistakenly executed on non-selected memory cells MC. For example, the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl can be set to a voltage which is half of the setting voltage Vset (Vset/2).

FIGS. **8** to **11** are cross-sectional views for explaining a voltage application state when a setting operation according to the present embodiment is executed on the memory cell MC.

As mentioned above, during the setting operation, the control circuit **16** applies the setting voltage Vset to the selected word line WL. Now, in the present embodiment, the higher a layer in which the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) are positioned, the larger the thicknesses La**1** to La**4** in the Z direction are made. Therefore, a wiring resistance of the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) changes depending on a position in the Z direction of the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). For example, the conductive layer **42***a* (word line WL**1**) has a largest wiring resistance, and the conductive layer **42***d* (word line WL**4**) has a smallest wiring resistance.

In the case where the wiring resistance of the conductive layers **42** (word lines WL) differs depending on a position in the Z direction, if a value of the setting voltage Vset is set to be identical in conductive layers (word lines WL) having different positions in the Z direction, then voltage applied to the selected memory cell MCs varies based on the position in the Z direction.

In contrast, in the present embodiment, as shown in FIGS. **8** to **11**, the control circuit **16** sets each of the values of the setting voltage Vset applied to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) to a different value. As shown in FIG. **8**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42***d* (word line WL**4**), the control circuit **16** applies a setting voltage Vset+ΔV**4** to the conductive layer **42***d* (word line WL**4**). As shown in FIG. **9**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42***c* (word line WL**3**), the control circuit **16** applies a setting voltage Vset+ΔV**3** to the conductive layer **42***c* (word line WL**3**). As shown in FIG. **10**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42***b* (word line WL**2**), the control circuit **16** applies a setting voltage Vset+ΔV**2** to the conductive layer **42***b* (word line WL**2**). As shown in FIG. **11**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42***a* (word line WL**1**), the control circuit **16** applies a setting voltage Vset+ΔV**1** to the conductive layer **42***a* (word line WL**1**).

At this time, values ΔV**1** to ΔV**4** are set such that ΔV**1**>ΔV**2**>ΔV**3**>ΔV**4**. That is, the setting voltages Vset+ΔV**1** to Vset+ΔV**4** are set such that the higher a layer in which the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) are positioned, the smaller an applied voltage during the setting operation becomes. Voltage values during the setting operation may be set such that the setting voltage Vset+ΔV**1** is about 1.3 times the setting voltage Vset+ΔV**4**.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the selected conductive layer **42** (selected word line WL) based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). By setting the setting voltage in this way, the voltage applied to the memory cell MC can be set substantially constant, even in conductive layers **42** (word lines WL) where the wiring resistance differs depending on the position in the Z direction. As a result, in the present embodiment, it is possible to suppress variation in the voltage applied to the selected memory cell MCs.

Second Embodiment

[Configuration]

Next, a semiconductor memory device according to a second embodiment will be described with reference to FIGS. **14** to **17**. The second embodiment has a similar configuration to the first embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment describes the resetting operation and the read operation.

[Method of Operation]

First, outlines of the resetting operation and the read operation will be described with reference to FIGS. **12** and **13**, and then a method of an operation of the semiconductor memory device according to the present embodiment will be described with reference to FIGS. **14** to **17**.

FIG. **12** is a cross-sectional view for explaining a voltage application state when the resetting operation is executed on the memory cell MC.

In the present embodiment, it is assumed that the resetting operation is executed on a selected memory cell MCs provided between the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**). In this case, the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**) become, respectively, a selected word line WL and a selected bit line BL. Moreover, the conductive layers **42***a* to **42***c* (word lines WL**1** to WL**3**) and the conductive layers **43** (bit lines BL**1** to BL**3**) become, respectively, non-selected word lines WL and non-selected bit lines BL.

The resetting operation is executed by applying to the selected memory cell MCs a resetting voltage such that the variable resistance element VR changes from the low-resistance state (set state) to the high-resistance state (reset state). During the resetting operation, the control circuit **16** applies a voltage Vresetg to the conductive layer **31** (selected global bit line GBL**4**) connected to the conductive layer **43** (selected bit line BL**4**), and applies a voltage Vn to the conductive layer **42***d* (selected word line WL**4**).

During the resetting operation, the control circuit **16** applies the non-selected word line voltage Vnwl to the conductive layers **42***a* to **42***c* (non-selected word lines WL**1** to WL**3**), and applies the non-selected global bit line voltage Vnblg to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Now, the control circuit **16** sets the select transistors STr**1** to STr**4** to an on state. Due to this, a resetting voltage Vreset is transferred to the conductive layer **43** (selected bit line BL**4**), and the non-selected bit line voltage Vnbl slightly lower than the non-selected global bit line voltage Vnblg is transferred to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) (note that Vreset>Vn). As a result, the resetting operation can be executed on the selected memory cell MCs only. Moreover, the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl are set to a voltage such that the resetting operation is not mistakenly executed on non-selected memory cells MC. For example, the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl can be set to a voltage which is half of the resetting voltage Vreset (Vreset/2).

FIG. **13** is a cross-sectional view for explaining a voltage application state when the read operation is executed on the memory cell MC. The read operation is executed by applying to the selected memory cell MCs a read voltage Vread for determining a resistance state of the variable resistance element VR. The read voltage Vread can be set to a voltage which is half of the resetting voltage Vreset (Vreset/2). In other respects, a method of voltage application of the read operation is similar to that of the resetting operation.

Now, the resetting operation and the read operation differ only in values of applied voltages, and are similar regarding a method of application of the voltages. The resetting operation will be described as an example below, but these operations may be applied also to the read operation.

FIGS. **14** to **17** are cross-sectional views for explaining a voltage application state when the resetting operation is executed according to the present embodiment on the memory cell MC.

As mentioned above, during the resetting operation, the control circuit **16** applies the resetting voltage Vreset to the selected bit line BL. Now, in the present embodiment, the higher a layer in which the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) are positioned, the larger the thicknesses La**1** to La**4** in the Z direction are made. Therefore, a wiring resistance of the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) changes depending on a position in the Z direction of the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). For example, the conductive layer **42***a* (word line WL**1**) has a largest wiring resistance, and the conductive layer **42***d* (word line WL**4**) has a smallest wiring resistance.

In the case where the wiring resistance of the conductive layers **42** (word lines WL) differs depending on a position in the Z direction, if a value of a word line voltage is set to be identical in conductive layers (word lines WL) having different positions in the Z direction, the voltage applied to the selected memory cell MCs varies based on the position in the Z direction.

In contrast, in the present embodiment, as shown in FIGS. **14** to **17**, the control circuit **16** sets each of values of the voltage applied to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**) to different values. As shown in FIG. **14**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42***d* (word line WL**4**), the control circuit **16** applies a voltage Vn+ΔV**8** to the conductive layer **42***d* (word line WL**4**). As shown in FIG. **15**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42***c* (word line WL**3**), the control circuit **16** applies a voltage Vn+ΔV**7** to the conductive layer **42***c* (word line WL**3**). As shown in FIG. **16**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42***b* (word line WL**2**), the control circuit **16** applies a voltage Vn+ΔV**6** to the conductive layer **42***b* (word line WL**2**). As shown in FIG. **17**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42***a* (word line WL**1**), the control circuit **16** applies a voltage Vn+ΔV**5** to the conductive layer **42***a* (word line WL**1**).

At this time, values ΔV**5** to ΔV**8** are set such that ΔV**8**>ΔV**7**>ΔV**6**>ΔV**5**. That is, the voltages Vn+ΔV**5** to Vn+ΔV**8** are set such that the higher a layer in which the conductive layers **42***a* to **42***d* are positioned, the larger an applied voltage during the resetting operation becomes. Voltage values during the resetting operation may be set such that the voltage Vn+ΔV**8** is about one tenth of the resetting voltage Vreset.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the selected conductive layer **42** (selected word line WL) based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). By setting the resetting voltage in this way, the voltage applied to the memory cell MC can be set substantially constant, even in conductive layers **42** (word lines WL) where the wiring resistance differs depending on the position in the Z direction. As a result, in the present embodiment, it is possible to suppress variation in the voltage applied to the selected memory cell MCs.

Third Embodiment

[Configuration]

Next, a semiconductor memory device according to a third embodiment will be described with reference to FIGS. **18**A and **18**B. The third embodiment has a similar configuration to the first embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment changes the voltages of the non-selected word lines WL and the non-selected bit lines BL during the setting operation.

[Method of Operation]

FIG. **18**A is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**). FIG. **18**B is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42***a* (word line WL**1**) and the conductive layer **43** (bit line BL**4**).

As mentioned above, during the setting operation, the control circuit **16** respectively applies the setting voltages Vset+ΔV**1** to Vset+ΔV**4** to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). Now, in the present embodiment, values of the voltage Vnwl and the voltage Vnbl applied to the non-selected word lines WL and the non-selected bit lines BL during the setting operation are changed according to the setting voltages Vset+ΔV**1** to Vset+ΔV**4**.

For example, as shown in FIG. **18**A, when the control circuit **16** applies the setting voltage Vset+ΔV**4** (for example, 3.0 V) to the conductive layer **42***d* (word line WL**4**) during the setting operation, a voltage value of a non-selected word line voltage Vnwl**1** is set to 1.5 V. In addition, a non-selected global bit line voltage Vnbl**1***g* is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Due to this, a voltage value of a non-selected bit line voltage Vnbl**1** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.5 V.

Moreover, as shown in FIG. **18**B, when the control circuit **16** applies the setting voltage Vset+ΔV**1** (for example, 3.4 V) to the conductive layer **42***a* (word line WL**1**) during the setting operation, a voltage value of a non-selected word line voltage Vnwl**2** is set to 1.7 V. In addition, a non-selected global bit line voltage Vnbl**2***g* is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Due to this, a voltage value of a non-selected bit line voltage Vnbl**2** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.7V. Now, a relationship Vnbl**2***g*>Vnbl**1***g* holds.

As mentioned above, during the setting operation, the control circuit **16** respectively applies the setting voltages Vset+ΔV**1** to Vset+ΔV**4** to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). In the present embodiment, values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl are changed corresponding to these setting voltages Vset+ΔV**1** to Vset+ΔV**4**. Only one of the values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl may be changed, or both may be changed.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the non-selected conductive layers **42** (word lines WL) or the conductive layers **31** (global bit lines GBL) connected to the non-selected conductive layers **43** (bit lines BL), based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). As a result, it is possible to suppress an excessive voltage being applied to non-selected memory cells MC connected between the selected word line WL and the non-selected bit lines BL. As a result, it is possible to suppress the setting operation being mistakenly executed on the non-selected memory cells MC.

Fourth Embodiment

[Configuration]

Next, a semiconductor memory device according to a fourth embodiment will be described with reference to FIGS. **19**A and **19**B. The fourth embodiment has a similar configuration to the first embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment changes the voltages of the non-selected word lines WL and the non-selected bit lines BL during the resetting operation.

[Method of Operation]

FIG. **19**A is a cross-sectional view for explaining a voltage application state when the resetting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**). FIG. **19**B is a cross-sectional view for explaining a voltage application state when the resetting operation is executed on the memory cell MC connected to the conductive layer **42***a* (word line WL**1**) and the conductive layer **43** (bit line BL**4**).

As mentioned above, during the resetting operation, the control circuit **16** respectively applies the voltages Vn+ΔV**5** to Vn+ΔV**8** to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). Now, in the present embodiment, values of the voltage Vnwl and the voltage Vnbl applied to the non-selected word lines WL and the non-selected bit lines BL during the resetting operation are changed according to the voltages Vn+ΔV**5** to Vn+ΔV**8**.

For example, as shown in FIG. **19**A, the control circuit **16** applies the voltage Vn+ΔV**8** (for example, 0.4 V) to the conductive layer **42***d* (word line WL**4**) during the resetting operation, a voltage value of the non-selected word line voltage Vnwl**1** is set to 1.7 V. In addition, the non-selected global bit line voltage Vnbl**1***g* is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers (non-selected bit lines BL**1** to BL**3**). Due to this, a voltage value of the non-selected bit line voltage Vnbl**1** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.7 V.

Moreover, as shown in FIG. **19**B, when the control circuit **16** applies the voltage Vn+ΔV**5** (for example, 0 V) to the conductive layer **42***a* (word line WL**1**) during the resetting operation, a voltage value of the non-selected word line voltage Vnwl**2** is set to 1.5 V. In addition, the non-selected global bit line voltage Vnbl**2***g* is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Due to this, a voltage value of the non-selected bit line voltage Vnbl**2** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.5V. Now, a relationship Vnbl**1***g*>Vnbl**2***g* holds.

As mentioned above, during the resetting operation, the control circuit **16** respectively applies the voltages Vn+ΔV**5** to Vn+ΔV**8** to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). In the present embodiment, values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl are changed corresponding to these voltages Vn+ΔV**5** to Vn+ΔV**8**. Only one of the values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl may be changed, or both may be changed.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the non-selected conductive layers **42** (word lines WL) or the conductive layers **31** (global bit lines GBL) connected to the non-selected conductive layers **43** (bit lines BL), based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). As a result, it is possible to suppress an excessive voltage being applied to the non-selected memory cells MC connected between the selected bit line BL and the non-selected word lines WL. As a result, it is possible to suppress the resetting operation being mistakenly executed on the non-selected memory cells MC.

Fifth Embodiment

[Configuration]

Next, a semiconductor memory device according to a fifth embodiment will be described with reference to FIGS. **20**A and **20**B. The fifth embodiment has a similar configuration to the first embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment changes the voltage of the selected word line WL during the setting operation.

[Method of Operation]

FIG. **20**A is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**1**). FIG. **20**B is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**).

As mentioned above, during the setting operation, the control circuit **16** applies the setting voltage Vset+ΔV**4** to the conductive layer **42***d* (word line WL**4**). Now, in the present embodiment, a value of the setting voltage Vset+ΔV**4** is changed based on the position of the selected memory cell MCs.

For example, as shown in FIG. **20**A, when the selected memory cell MCs is at a position close to the row decoder **12**, the control circuit **16** applies the setting voltage Vset+ΔV**4** to the conductive layer **42***d* (word line WL**4**). On the other hand, as shown in FIG. **20**B, when the selected memory cell MCs is at a position far from the row decoder **12**, the control circuit **16** applies a setting voltage Vset+ΔV**4**'(ΔV**4**'>ΔV**4**) to the conductive layer **42***d* (word line WL**4**).

In such a way, in the present embodiment, the voltage of the selected word line WL is changed based on a position in the X direction of the selected memory cell MCs. Note that a similar operation can be executed also when the setting operation is executed on the memory cells MC connected to each of the conductive layers **42***c* to **42***a* (word lines WL**3** to WL**1**) other than the conductive layer **42***d* (word line WL**4**). Moreover, although a description is omitted, the voltage of the selected word line WL can be changed based on the position in the X direction of the selected memory cell MCs also in the resetting operation and the read operation.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the selected conductive layer **42** (selected word line WL) based on the position in the X direction of the selected memory cell MCs. Even in an identical selected word line WL, when a distance from the row decoder **12** to the selected memory cell MCs differs, an amount of voltage drop in the selected word line WL differs. By setting the value of the setting voltage Vset applied to the selected word line WL in this way, the voltage applied to the selected memory cell MCs can be set to be substantially constant. As a result, in the present embodiment, it is possible to suppress variation in the voltage applied to the selected memory cell MCs.

Sixth Embodiment

[Configuration]

Next, a semiconductor memory device according to a sixth embodiment will be described with reference to FIGS. **21** to **25**. FIG. **21** shows the memory layer **40** as seen from the Y direction. Note that in FIG. **21**, the interlayer insulating layers **41**_a_ to **41**_d_ and the variable resistance layer **44** are omitted. A plane in FIG. **21** corresponds to an F**6**-F**6** cross-section of FIG. **3**.

In the sixth embodiment, as shown in FIG. **21**, the conductive layer **43** is formed in an inverse tapered shape as seen from the Y direction, and a width in the X direction of a side surface in the Y direction of the conductive layer **43** becomes gradually smaller proceeding in a –Z direction (downward direction of FIG. **21**). That is, the width in the X direction of the side surface in the Y direction of the conductive layer **43** at a first position is larger than the width in the X direction of the side surface in the Y direction of the conductive layer **43** at a second position lower than the first position. For example, as shown in FIG. **21**, if a width of the conductive layer **43** at a position corresponding to the conductive layer **42**_a_ is assumed to be Xb**1**, a width of the conductive layer **43** at a position corresponding to the conductive layer **42**_b_ is assumed to be Xb**2**, a width of the conductive layer **43** at a position corresponding to the conductive layer **42**_c_ is assumed to be Xb**3**, and a width of the conductive layer **43** at a position corresponding to the conductive layer **42**_d_ is assumed to be Xb**4**, then Xb**1**<Xb**2**<Xb**3**<Xb**4**. Note that this inverse tapered shape of the conductive layer **43** can be formed by adjusting an etching condition during manufacturing. Now, if thicknesses in the Z direction of the conductive layers **42**_a_ to **42**_d_ are assumed to be substantially uniform, then a facing area between the conductive layer **42**_d_ and the conductive layer **43** is largest, and a facing area between the conductive layer **42**_a_ and the conductive layer **43** is smallest. As a result, variation occurs in characteristics of the variable resistance element VR formed between the conductive layers **42**_a_ to **42**_d_ (word lines WL**1** to WL**4**) and the conductive layer **43** (bit line BL).

Accordingly, in the present embodiment, as shown in FIG. **21**, the lower a layer in which the conductive layers **42**_a_ to **42**_d_ are positioned, the larger the thicknesses Lb**1** to Lb**4** in the Z direction are made in accordance with the above-described shape of the conductive layer **43**. Specifically, the thickness Lb**1** in the Z direction of the conductive layer **42**_a_ is larger than the thickness Lb**2** in the Z direction of the conductive layer **42**_b_ in a layer above the conductive layer **42**_a_. Similarly, the thickness Lb**2** in the Z direction of the conductive layer **42**_b_ is larger than the thickness Lb**3** in the Z direction of the conductive layer **42**_c_ in a layer above the conductive layer **42**_b_, and the thickness Lb**3** in the Z direction of the conductive layer **42**_c_ is larger than the thickness Lb**4** in the Z direction of the conductive layer **42**_d_ in a layer above the conductive layer **42**_c_. Therefore, facing areas between the conductive layers **42**_a_ to **42**_d_ and the conductive layer **43** can be made substantially constant. As a result, in the present embodiment, it is possible to suppress variation in characteristics of the variable resistance element VR.

[Method of Operation]

Next, a method of an operation of the semiconductor memory device according to the present embodiment will be described. In the present embodiment, details of a method of voltage application during the setting operation will be described.

FIGS. **22** to **25** are cross-sectional views for explaining a voltage application state when the setting operation is executed on the memory cell MC.

As mentioned above, during the setting operation, the control circuit **16** applies the setting voltage Vset to the selected word line WL. Now, in the present embodiment, the lower a layer in which the conductive layers **42**_a_ to **42**_d_ (word lines WL**1** to WL**4**) are positioned, the larger the thicknesses Lb**1** to Lb**4** in the Z direction are made. Therefore, a wiring resistance of the conductive layers **42**_a_ to **42**_d_ (word lines WL**1** to WL**4**) changes depending on the position in the Z direction of the conductive layers **42**_a_ to **42**_d_ (word lines WL**1** to WL**4**). For example, the conductive layer **42**_d_ (word line WL**4**) has a largest wiring resistance, and the conductive layer **42**_a_ (word line WL**1**) has a smallest wiring resistance.

In the case where the wiring resistance of the conductive layers **42** (word lines WL) differs depending on the position in the Z direction, if the value of the setting voltage Vset is set to be identical in conductive layers **42** (word lines WL) having different positions in the Z direction, then the voltage applied to the selected memory cell MCs varies based on the position in the Z direction.

In contrast, in the present embodiment, as shown in FIGS. **22** to **25**, the control circuit **16** sets each of the values of the setting voltage Vset applied to the conductive layers **42**_a_ to **42**_d_ (word lines WL**1** to WL**4**) to a different value. As shown in FIG. **22**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42**_d_ (word line WL**4**), the control circuit **16** applies the setting voltage Vset+ΔV**4** to the conductive layer **42**_d_ (word line WL**4**). As shown in FIG. **23**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42**_c_ (word line WL**3**), the control circuit **16** applies the setting voltage Vset+ΔV**3** to the conductive layer **42**_c_ (word line WL**3**). As shown in FIG. **24**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42**_b_ (word line WL**2**), the control circuit **16** applies the setting voltage Vset+ΔV**2** to the conductive layer **42**_b_ (word line WL**2**). As shown in FIG. **25**, during the setting operation of the selected memory cell MCs connected to the conductive layer **42**_a_ (word line WL**1**), the control circuit **16** applies the setting voltage Vset+ΔV**1** to the conductive layer **42**_a_ (word line WL**1**).

At this time, the values ΔV**1** to ΔV**4** are set such that ΔV**4**>ΔV**3**>ΔV**2**>ΔV**1**. That is, the setting voltages Vset+ΔV**1** to Vset+ΔV**4** are set such that the lower a layer in which the conductive layers **42**_a_ to **42**_d_ (word lines WL**1** to WL**4**) are positioned, the smaller the applied voltage during the setting operation becomes. The voltage values during the setting operation may be set such that the setting voltage Vset+ΔV**4** is about 1.3 times the setting voltage Vset+ΔV**1**.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the selected conductive layer **42** (selected word line WL) based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). By setting the setting voltage in this way, the voltage applied to the memory cell MC can be set substantially constant, even in conductive layers **42** (word lines WL) where the wiring resistance differs depending on the position in the Z direction. As a result, in the present embodiment, it is possible to suppress variation in the voltage applied to the selected memory cell MCs.

Seventh Embodiment

[Configuration]

Next, a semiconductor memory device according to a seventh embodiment will be described with reference to FIGS. **26** to **29**. The seventh embodiment has a similar configuration to the sixth embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment describes the resetting operation.

[Method of Operation]

In the present embodiment, details of a method of voltage application during the resetting operation will be described.

FIGS. **26** to **29** are cross-sectional views for explaining a voltage application state when the resetting operation is executed on the memory cell MC.

As mentioned above, during the resetting operation, the control circuit **16** applies the resetting voltage Vreset to the selected bit line BL. Now, in the present embodiment, the lower a layer in which the conductive layers **42**a to **42**d (word lines WL**1** to WL**4**) are positioned, the larger the thicknesses Lb**1** to Lb**4** in the Z direction are made. Therefore, a wiring resistance of the conductive layers **42**a to **42**d (word lines WL**1** to WL**4**) changes depending on the position in the Z direction of the conductive layers **42**a to **42**d (word lines WL**1** to WL**4**). For example, the conductive layer **42**d (word line WL**4**) has a largest wiring resistance, and the conductive layer **42**a (word line WL**1**) has a smallest wiring resistance.

In the case where the wiring resistance of the conductive layers **42** (word lines WL) differs depending on the position in the Z direction, if the value of the word line voltage is set to be identical in conductive layers **42** (word lines WL) having different positions in the Z direction, then the voltage applied to the selected memory cell MCs varies based on the position in the Z direction.

In contrast, in the present embodiment, as shown in FIGS. **26** to **29**, the control circuit **16** sets each of the values of the voltage applied to the conductive layers **42**a to **42**d (word lines WL**1** to WL**4**) to a different value. As shown in FIG. **26**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42**d (word line WL**4**), the control circuit **16** applies the voltage Vn+ΔV**8** to the conductive layer **42**d (word line WL**4**). As shown in FIG. **27**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42**c (word line WL**3**), the control circuit **16** applies the voltage Vn+ΔV**7** to the conductive layer **42**c (word line WL**3**). As shown in FIG. **28**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42**b (word line WL**2**), the control circuit **16** applies the voltage Vn+ΔV**6** to the conductive layer **42**b (word line WL**2**). As shown in FIG. **29**, during the resetting operation of the selected memory cell MCs connected to the conductive layer **42**a (word line WL**1**), the control circuit **16** applies the voltage Vn+ΔV**5** to the conductive layer **42**a (word line WL**1**).

At this time, the values ΔV**5** to ΔV**8** are set such that ΔV**5**>ΔV**6**>ΔV**7**>ΔV**8**. That is, the voltages Vn+ΔV**5** to Vn+ΔV**8** are set such that the lower a layer in which the conductive layers **42**a to **42**d are positioned, the larger the applied voltage during the resetting operation becomes. The voltage values during the resetting operation may be set such that the voltage Vn+ΔV**5** is about one tenth of the resetting voltage Vreset.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the selected conductive layer **42** (selected word line WL) based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). By setting the resetting voltage in this way, the voltage applied to the memory cell MC can be set substantially constant, even in conductive layers **42** (word lines WL) where the wiring resistance differs depending on the position in the Z direction. As a result, in the present embodiment, it is possible to suppress variation in the voltage applied to the selected memory cell MCs.

Eighth Embodiment

[Configuration]

Next, a semiconductor memory device according to an eighth embodiment will be described with reference to FIGS. **30**A and **30**B. The eighth embodiment has a similar configuration to the sixth embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment changes the voltages of the non-selected word lines WL and the non-selected bit lines BL during the setting operation.

[Method of Operation]

FIG. **30**A is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42**d (word line WL**4**) and the conductive layer **43** (bit line BL**4**). FIG. **30**B is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42**a (word line WL**1**) and the conductive layer **43** (bit line BL**4**).

As mentioned above, during the setting operation, the control circuit **16** respectively applies the setting voltages Vset+ΔV**1** to Vset+ΔV**4** to the conductive layers **42**a to **42**d (word lines WL**1** to WL**4**). Now, in the present embodiment, the values of the voltage Vnwl and the voltage Vnbl applied to the non-selected word lines WL and the non-selected bit lines BL during the setting operation are changed according to the setting voltages Vset+ΔV**1** to Vset+ΔV**4**.

For example, as shown in FIG. **30**A, when the control circuit **16** applies the setting voltage Vset+ΔV**4** (for example, 3.4 V) to the conductive layer **42**d (word line WL**4**), the voltage value of the non-selected word line voltage Vnwl**1** is set to 1.7 V. In addition, the non-selected global bit line voltage Vnbl**1**g is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers (non-selected bit lines BL**1** to BL**3**). Due to this, the voltage value of the non-selected bit line voltage Vnbl**1** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.7 V.

Moreover, as shown in FIG. **30**B, when the control circuit **16** applies the setting voltage Vset+ΔV**1** (for example, 3.0 V) to the conductive layer **42**a (word line WL**1**) during the setting operation, the voltage value of the non-selected word line voltage Vnwl**2** is set to 1.5 V. In addition, the non-selected global bit line voltage Vnbl**2**g is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Due to this, the voltage value of the non-selected bit line voltage Vnbl**2** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.5V. Now, a relationship Vnbl**1**g>Vnbl**2**g holds.

As mentioned above, during the setting operation, the control circuit **16** respectively applies the setting voltages Vset+ΔV**1** to Vset+ΔV**4** to the conductive layers **42**a to **42**d (word lines WL**1** to WL**4**). In the present embodiment, the values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl are changed corresponding to these setting voltages Vset+ΔV**1** to Vset+ΔV**4**. Only one of the values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl may be changed, or both may be changed.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the non-selected conductive layers **42** (word lines WL) or the conductive layers **31** (global bit lines GBL) connected to the non-selected conductive layers **43** (bit lines BL), based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). As a result, it is possible to suppress an excessive voltage being applied to the non-selected memory cells MC connected between the selected word line WL and the non-selected bit lines BL. As a result, it is possible to suppress the setting operation being mistakenly executed on the non-selected memory cells MC.

Ninth Embodiment

[Configuration]

Next, a semiconductor memory device according to a ninth embodiment will be described with reference to FIGS. **31**A and **31**B. The ninth embodiment has a similar configuration to the sixth embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment changes the voltages of the non-selected word lines WL and the non-selected bit lines BL during the resetting operation.

[Method of Operation]

FIG. **31**A is a cross-sectional view for explaining a voltage application state when the resetting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**). FIG. **31**B is a cross-sectional view for explaining a voltage application state when the resetting operation is executed on the memory cell MC connected to the conductive layer **42***a* (word line WL**1**) and the conductive layer **43** (bit line BL**4**).

As mentioned above, during the resetting operation, the control circuit **16** respectively applies the voltages Vn+ΔV**5** to Vn+ΔV**8** to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). Now, in the present embodiment, the values of the voltage Vnwl and the voltage Vnbl applied to the non-selected word lines WL and the non-selected bit lines BL during the resetting operation are changed according to the voltages Vn+ΔV**5** to Vn+ΔV**8**.

For example, as shown in FIG. **31**A, when the control circuit **16** applies the voltage Vn+ΔV**8** (for example, 0 V) to the conductive layer **42***d* (word line WL**4**) during the resetting operation, the voltage value of the non-selected word line voltage Vnwl**1** is set to 1.5 V. In addition, the non-selected global bit line voltage Vnbl**1***g* is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Due to this, the voltage value of the non-selected bit line voltage Vnbl**1** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.5 V.

Moreover, as shown in FIG. **31**B, when the control circuit **16** applies the voltage Vn+ΔV**5** (for example, 0.4 V) to the conductive layer **42***a* (word line WL**1**), the voltage value of the non-selected word line voltage Vnwl**2** is set to 1.7 V. In addition, the non-selected global bit line voltage Vnbl**2***g* is applied to the conductive layers **31** (non-selected global bit lines GBL**1** to GBL**3**) connected to the conductive layers **43** (non-selected bit lines BL**1** to BL**3**). Due to this, the voltage value of the non-selected bit line voltage Vnbl**2** of the conductive layers **43** (non-selected bit lines BL**1** to BL**3**) is set to approximately 1.7 V. Now, a relationship Vnbl**2***g*>Vnbl**1***g* holds.

As mentioned above, during the resetting operation, the control circuit **16** respectively applies the voltages Vn+ΔV**5** to Vn+ΔV**8** to the conductive layers **42***a* to **42***d* (word lines WL**1** to WL**4**). In the present embodiment, the values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl are changed corresponding to these voltages Vn+ΔV**5** to Vn+ΔV**8**. Only one of the values of the non-selected word line voltage Vnwl and the non-selected bit line voltage Vnbl may be changed, or both may be changed.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the non-selected conductive layers **42** (word lines WL) or the conductive layers **31** (global bit lines GBL) connected to the non-selected conductive layers **43** (bit lines BL), based on the position in the Z direction of the selected conductive layer **42** (selected word line WL). As a result, it is possible to suppress an excessive voltage being applied to the non-selected memory cells MC connected between the selected bit line BL and the non-selected word lines WL. As a result, it is possible to suppress the resetting operation being mistakenly executed on the non-selected memory cells MC.

Tenth Embodiment

[Configuration]

Next, a semiconductor memory device according to a tenth embodiment will be described with reference to FIGS. **32**A and **32**B. The tenth embodiment has a similar configuration to the sixth embodiment, hence in the present embodiment, a description of the configuration will be omitted. The present embodiment changes the voltage of the selected word line WL during the setting operation.

[Method of Operation]

FIG. **32**A is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**1**). FIG. **32**B is a cross-sectional view for explaining a voltage application state when the setting operation is executed on the memory cell MC connected to the conductive layer **42***d* (word line WL**4**) and the conductive layer **43** (bit line BL**4**).

As mentioned above, during the setting operation, the control circuit **16** applies the setting voltage Vset+ΔV**4** to the conductive layer **42***d* (word line WL**4**). Now, in the present embodiment, the value of the setting voltage Vset+ΔV**4** is changed based on the position of the selected memory cell MCs.

For example, as shown in FIG. **32**A, when the selected memory cell MCs is at a position close to the row decoder **12**, the control circuit **16** applies the setting voltage Vset+ΔV**4** to the conductive layer **42***d* (word line WL**4**). On the other hand, as shown in FIG. **32**B, when the selected memory cell MCs is at a position far from the row decoder **12**, the control circuit **16** applies the setting voltage Vset+ΔV**4**'(ΔV**4**'>ΔV**4**) to the conductive layer **42***d* (word line WL**4**).

In such a way, in the present embodiment, the voltage of the selected word line WL is changed based on the position in the X direction of the selected memory cell MCs. Note that a similar operation can be executed also when the setting operation is executed on the memory cells MC connected to each of the conductive layers **42***c* to **42***a* (word lines WL**3** to WL**1**) other than the conductive layer **42***d* (word line WL**4**). Moreover, although a description is omitted, the voltage of the selected word line WL can be changed based on the position in the X direction of the selected memory cell MCs also in the resetting operation and the read operation.

[Advantages]

In the operation of the present embodiment, the control circuit changes the value of the voltage applied to the selected conductive layer **42** (selected word line WL) based on the position in the X direction of the selected memory cell MCs. Even in an identical selected word line WL, when the distance from the row decoder **12** to the selected memory cell MCs differs, the amount of voltage drop in the selected word line WL differs. By setting the value of the setting voltage Vset applied to the selected word line WL in this way, the voltage applied to the selected memory cell MCs can be set to be substantially constant. As a result, in the present embodiment, it is possible to suppress variation in the voltage applied to the selected memory cell MCs.

[Other]

While certain embodiments have been described, these embodiments have been presented byway of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A semiconductor memory device, comprising a memory cell array and a control circuit,

the memory cell array including:

a plurality of first conductive layers that are stacked in a first direction perpendicular to a substrate and extend in a second direction parallel to the substrate;

a memory layer provided on a side surface of the plurality of the first conductive layers; and

a second conductive layer that extends in the first direction and includes a first side surface that contacts the side surface of the plurality of the first conductive layers via the memory layer,

a first width in the second direction of the first side surface of the second conductive layer at a first position in the first direction being smaller than a second width in the second direction of the first side surface of the second conductive layer at a second position in the first direction nearer to the substrate than the first position,

a first thickness in the first direction of the first conductive layer disposed at the first position being larger than a second thickness in the first direction of the first conductive layer disposed at the second position,

the control circuit being configured to apply a first voltage to a selected first conductive layer of the first conductive layers and provide a second voltage to the second conductive layer, and

the control circuit being configured to, when the control circuit applies the first voltage to the selected first conductive layer, change a value of the first voltage based on a relative position in the first direction of the selected first conductive layer.

2. The semiconductor memory device according to claim **1**, wherein

the control circuit is configured to, when the control circuit applies a third voltage to a non-selected first conductive layer of the first conductive layers, change a value of the third voltage based on a relative position in the first direction of the selected first conductive layer.

3. The semiconductor memory device according to claim **1**, wherein

a plurality of the second conductive layers are disposed in the second direction,

the control circuit is configured to apply the second voltage to a selected second conductive layer of the second conductive layers, and

the control circuit is configured to, when the control circuit provides a fourth voltage to a non-selected second conductive layer of the second conductive layers, change a value of the fourth voltage based on a relative position in the first direction of the selected first conductive layer.

4. The semiconductor memory device according to claim **1**, wherein

a plurality of the second conductive layers are disposed in the second direction,

the control circuit is configured to apply the second voltage to a selected second conductive layer of the second conductive layers, and

the control circuit is configured to, when the control circuit applies the first voltage to the selected first conductive layer, change a value of the first voltage based on a relative position in the second direction of the selected second conductive layer.

5. The semiconductor memory device according to claim **1**, wherein

the memory cell array further comprises:

a third conductive layer that extends in a third direction orthogonal to the first direction and the second direction; and

a select transistor that contacts an upper surface of the third conductive layer and a lower surface of the second conductive layer, and

the control circuit is configured to provide the second voltage to the second conductive layer by applying a fifth voltage to the third conductive layer.

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